Switch-mode Power Rectifiers

MBR2535CTG, MBR2545CTG

The MBR2535CTG/45CTG series uses the Schottky Barrier principle with a platinum barrier metal. These state−of−the−art devices have the following features:

Features

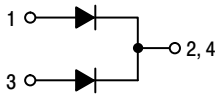
- Guardring for Stress Protection
- Low Forward Voltage
- 175°C Operating Junction Temperature
- These are Pb−Free Devices*

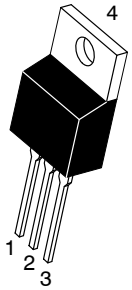
Mechanical Characteristics

- Case: Epoxy, Molded
- Epoxy Meets UL 94 V−0 @ 0.125 in
- Weight: 1.9 Grams (Approximately)
- Finish: All External Surfaces Corrosion Resistant and Terminal Leads are Readily Solderable
- Lead Temperature for Soldering Purposes: 260°C Max. for 10 Seconds

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

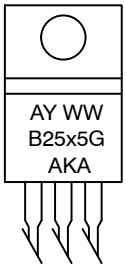
SCHOTTKY BARRIER RECTIFIERS
30 AMPERES
35 and 45 VOLTS





TO−220
CASE 221A
STYLE 6

MARKING DIAGRAM



A	= Assembly Location
Y	= Year
WW	= Work Week
B25x5	= Device Code
x	= 3 or 4
G	= Pb−Free Package
AKA	= Diode Polarity

ORDERING INFORMATION

Device	Package	Shipping
MBR2535CTG	TO−220 (Pb−Free)	50 Units/Rail
MBR2545CTG	TO−220 (Pb−Free)	50 Units/Rail

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage MBR2535CTG MBR2545CTG	V_{RRM} V_{RWM} V_R	 35 45	V
Average Rectified Forward Current (Rated V_R, T_C = 160°C) Per Device Per Diode	$I_{F(AV)}$	 30 15	A
Peak Repetitive Forward Current per Diode Leg (Rated V_R, Square Wave, 20 kHz, T_C = 150°C)	I_{FRM}	 30	A
Non−Repetitive Peak Surge Current per Diode Leg (Surge Applied at Rated Load Conditions, Halfwave, Single Phase, 60 Hz)	I_{FSM}	 150	A
Peak Repetitive Reverse Surge Current (2.0 μs, 1.0 kHz)	I_{RRM}	1.0	A
Storage Temperature Range	T_{stg}	−65 to +175	°C
Operating Junction Temperature (Note 1)	T_J	−65 to +175	°C
Voltage Rate of Change (Rated V_R)	dv/dt	10,000	V/μs
ESD Ratings: Machine Model = C Human Body Model = 3B	ESD	 > 400 > 8000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The heat generated must be less than the thermal conductivity from Junction−to−Ambient: $dP_D/dT_J < 1/R_{\theta JA}$.

THERMAL CHARACTERISTICS (Per Leg)

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction−to−Case Junction−to−Ambient (Note 2)	 $R_{\theta JC}$ $R_{\theta JA}$	 1.5 50	°C/W

2. When mounted using minimum recommended pad size on FR−4 board.

ELECTRICAL CHARACTERISTICS (Per Diode)

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_F	Instantaneous Forward Voltage (Note 3)	I_F = 15 A, T_J = 25°C I_F = 15 A, T_J = 125°C I_F = 30 A, T_J = 25°C I_F = 30 A, T_J = 125°C	– – – –	– 0.50 – 0.65	0.62 0.57 0.82 0.72	V
I_R	Instantaneous Reverse Current (Note 3)	Rated dc Voltage, T_J = 25°C Rated dc Voltage, T_J = 125°C	– –	– 9.0	0.2 25	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

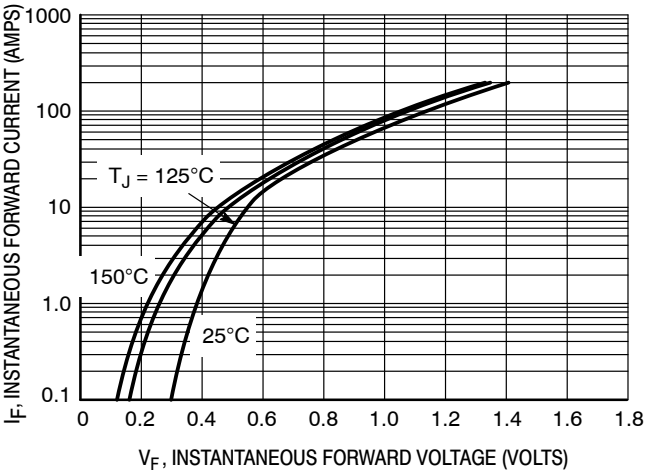


Figure 1. Typical Forward Voltage, Per Leg

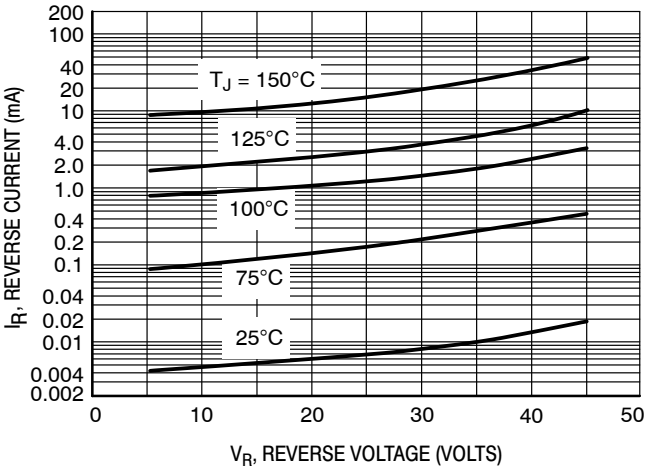


Figure 2. Typical Reverse Current, Per Leg

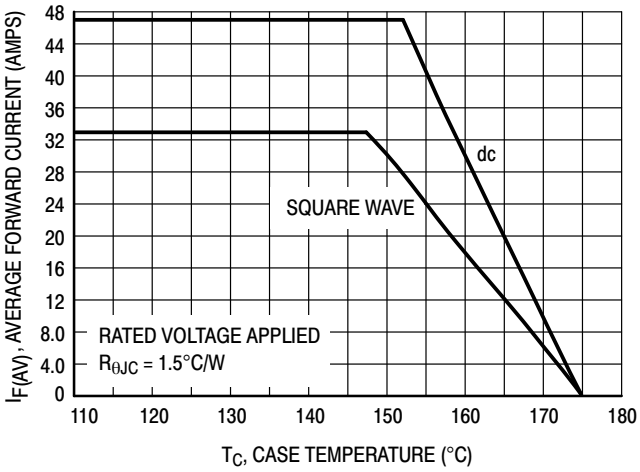


Figure 3. Current Derating, Per Device

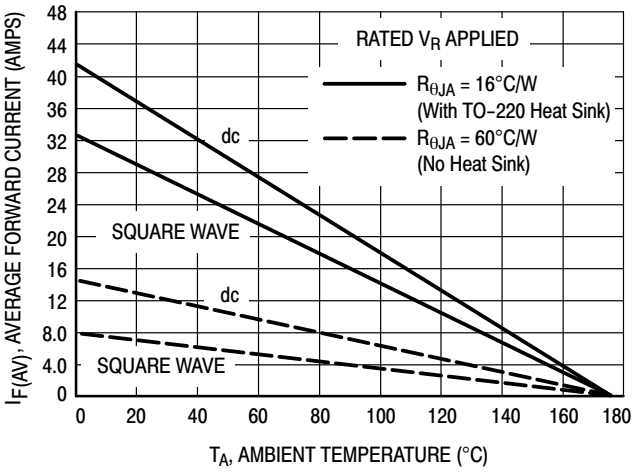


Figure 4. Current Derating, Per Device

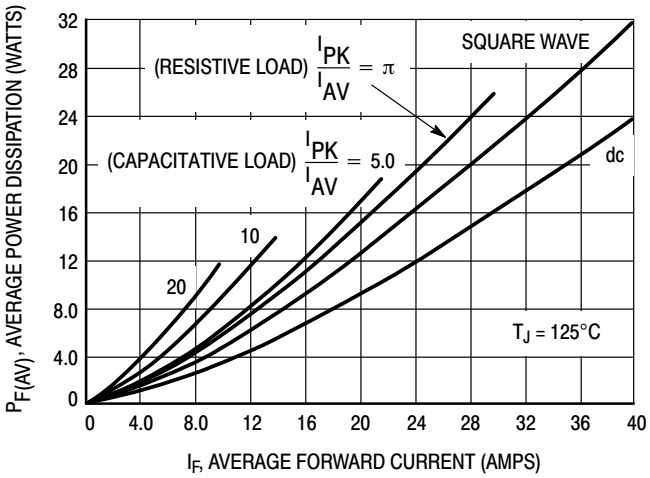
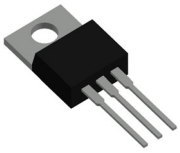
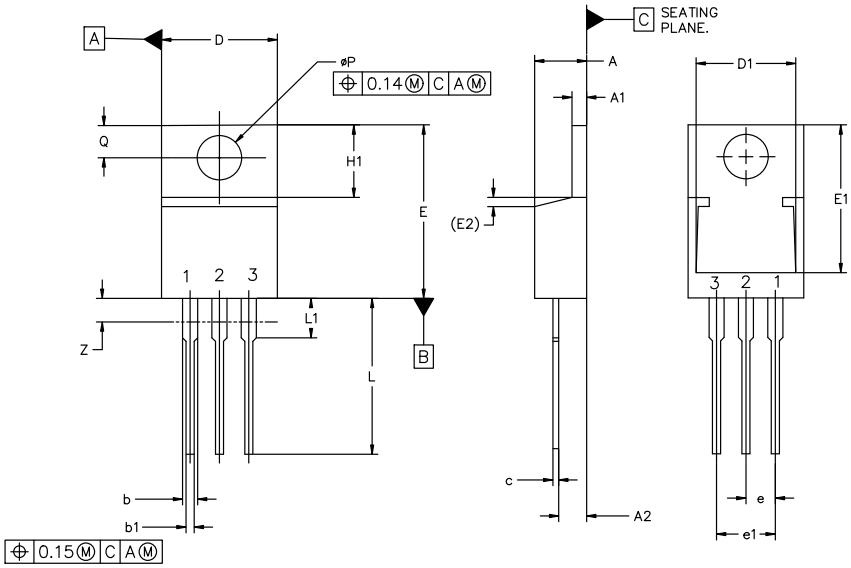


Figure 5. Forward Power Dissipation



TO−220−3 10.10x15.12x4.45, 2.54P
CASE 221A
ISSUE AL

DATE 05 FEB 2025



MILLIMETERS			
DIM	MIN	NOM	MAX
A	4.07	4.45	4.83
A1	1.15	1.28	1.41
A2	2.04	2.42	2.79
b	1.15	1.34	1.52
b1	0.64	0.80	0.96
c	0.36	0.49	0.61
D	9.66	10.10	10.53
D1	8.43	8.63	8.83
E	14.48	15.12	15.75
E1	12.58	12.78	12.98
E2	1.27 REF		

MILLIMETERS			
DIM	MIN	NOM	MAX
e	2.42	2.54	2.66
e1	4.83	5.08	5.33
H1	5.97	6.22	6.47
L	12.70	13.49	14.27
L1	2.80	3.45	4.10
Q	2.54	2.79	3.04
øP	3.60	3.85	4.09
Z	–.––	–.––	3.48

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

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