

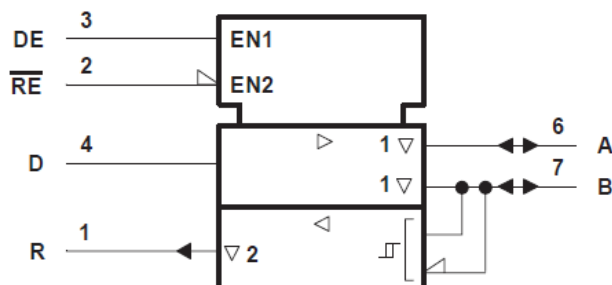
# SNx5ALS176, SN75ALS176A, and SN75ALS176B Differential Bus Transceivers

## 1 Features

- Meet or exceed the requirements of TIA/EIA-422-B, TIA/EIA-485-A<sup>1</sup> and ITU recommendations V.11 and X.27
- Operate at data rates up to 35 Mbaud
- Four skew limits available:
  - SN65ALS176: 15 ns
  - SN75ALS176: 10 ns
  - SN75ALS176A: 7.5 ns
  - SN75ALS176B: 5 ns
- Designed for multipoint transmission on long bus lines in noisy environments
- Low supply-current requirements: 30 mA max
- Wide positive and negative input/output bus-voltage ranges
- Thermal shutdown protection
- Driver positive and negative current limiting
- Receiver input hysteresis
- Glitch-free power-up and power-down protection
- Receiver open-circuit fail-safe design

## 2 Description

The SN65ALS176 and SN75ALS176 series differential bus transceivers are designed for bidirectional data communication on multipoint bus transmission lines. The devices are designed for balanced transmission lines and meet TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendations V.11 and X.27.



A. This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**Logic Symbol**

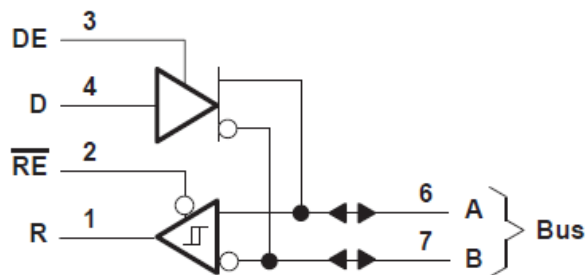
The SN65ALS176 and SN75ALS176 series combine a 3-state, differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be connected together externally to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus when the driver is disabled or  $V_{CC} = 0$ . This port features wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications.

The SN65ALS176 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . The SN75ALS176 series is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

### Package Information

| PART NUMBER | PACKAGE <sup>(1)</sup> | BODY SIZE (NOM)   |
|-------------|------------------------|-------------------|
| SNx5ALS176  | D (SOIC)               | 4.9 mm x 3.91 mm  |
|             | P (PDIP)               | 9.81 mm x 6.35 mm |
| SN75ALS176A | D (SOIC)               | 4.9 mm x 3.91 mm  |
|             | P (PDIP)               | 9.81 mm x 6.35 mm |
| SN75ALS176B | D (SOIC)               | 4.9 mm x 3.91 mm  |
|             | P (PDIP)               | 9.81 mm x 6.35 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



**Logic Diagram (Positive Logic)**

<sup>1</sup> These devices meet or exceed the requirements of TIA/EIA-485-A, except for the Generator Contention Test (para. 3.4.2) and the Generator Current Limit (para. 3.4.3). The applied test voltage ranges are  $-6\text{ V}$  to  $8\text{ V}$  for the SN75ALS176, SN75ALS176A, and SN75ALS176B and  $-4\text{ V}$  to  $8\text{ V}$  for the SN65ALS180.



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## 3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision H (June 2000) to Revision I (January 2023)</b>                | <b>Page</b> |
|----------------------------------------------------------------------------------------|-------------|
| • Changed the document to the latest TI format.....                                    | 1           |
| • Deleted the Package thermal impedance from the <i>Absolute Maximum Ratings</i> ..... | 4           |
| • Added the <i>Thermal Information</i> table.....                                      | 4           |
| • Changed the <i>Typical Characteristics</i> graphs.....                               | 9           |

## 4 Pin Configuration and Functions

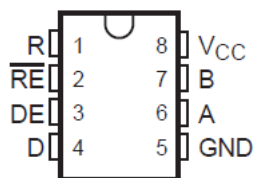


**Figure 4-1. D or P Package (Top View)**

**Table 4-1. Pin Functions**

| NO | Name            | Type   | Description                                          |
|----|-----------------|--------|------------------------------------------------------|
| 1  | R               | O      | Receive data output                                  |
| 2  | $\overline{RE}$ | I      | Receiver enable, active low                          |
| 3  | DE              | i      | Driver enable, active high                           |
| 4  | D               | I      | Driver data input                                    |
| 5  | GND             | GND    | Local device ground                                  |
| 6  | A               | I/O    | Driver output or receiver input (complementary to B) |
| 7  | B               | I/O    | Driver output or receiver input (complementary to A) |
| 8  | $V_{CC}$        | SUPPLY | 4.75-V to 5.25-V supply                              |

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |                                                              | MIN | MAX | UNIT |
|------------------|--------------------------------------------------------------|-----|-----|------|
| V <sub>CC</sub>  | Supply voltage <sup>(2)</sup>                                |     | 7   | V    |
|                  | Voltage range at any bus terminal                            | -7  | 12  | V    |
| V <sub>I</sub>   | Enable input voltage                                         |     | 5.5 | V    |
|                  | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds |     | 260 | °C   |
| T <sub>stg</sub> | Storage temperature range                                    | -65 | 150 | °C   |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

### 5.2 Recommended Operating Conditions

(unless otherwise noted)

|                                   |                                                               |                   | MIN  | NOM | MAX  | UNIT |
|-----------------------------------|---------------------------------------------------------------|-------------------|------|-----|------|------|
| V <sub>CC</sub>                   | Supply voltage                                                |                   | 4.75 | 5   | 5.25 | V    |
| V <sub>I</sub> or V <sub>IC</sub> | Input voltage at any bus terminal (separately or common mode) |                   |      |     | 12   | V    |
|                                   |                                                               |                   |      |     | -7   | V    |
| V <sub>IH</sub>                   | High-level input voltage                                      | D, DE, and RE     | 2    |     |      | V    |
| V <sub>IL</sub>                   | Low-level input voltage                                       | D, DE, and RE     |      |     | 0.8  | V    |
| V <sub>ID</sub>                   | Differential input voltage <sup>(1)</sup>                     |                   |      |     | ±12  | V    |
| I <sub>OH</sub>                   | High-level output current                                     | Driver            |      |     | -60  | mA   |
|                                   |                                                               | Receiver          |      |     | -400 | µA   |
| I <sub>OL</sub>                   | Low-level output current                                      | Driver            |      |     | 60   | mA   |
|                                   |                                                               | Receiver          |      |     | 8    | mA   |
| T <sub>A</sub>                    | Operating free-air temperature                                | SN65ALS176        | -40  |     | 85   | °C   |
|                                   |                                                               | SN75ALS176 series | 0    |     | 70   | °C   |

- (1) Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

### 5.3 Thermal Information

|                               |                                              | P (PDIP) | D (SOIC)<br>SN65 Devices | D (SOIC)<br>SN75 Devices | UNIT |
|-------------------------------|----------------------------------------------|----------|--------------------------|--------------------------|------|
| THERMAL METRIC <sup>(1)</sup> |                                              | 8-Pins   | 8-Pins                   | 8-Pin                    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 65.7     | 116.7                    | 110                      | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case thermal resistance          | 54.7     | 56.3                     | 44.1                     | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 42.1     | 63.4                     | 53.5                     | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 23       | 8.8                      | 4.8                      | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 41.7     | 62.6                     | 52.7                     | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | N/A      | N/A                      | N/A                      | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

## 5.4 Electrical Characteristics - Driver

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

| PARAMETER         |                                                                   | TEST CONDITIONS <sup>(1)</sup>    |                       | MIN                                       | TYP <sup>(2)</sup> | MAX     | UNIT |
|-------------------|-------------------------------------------------------------------|-----------------------------------|-----------------------|-------------------------------------------|--------------------|---------|------|
| V <sub>IK</sub>   | Input clamp voltage                                               | I <sub>I</sub> = -18 mA           |                       |                                           |                    | -1.5    | V    |
| V <sub>O</sub>    | Output voltage                                                    | I <sub>O</sub> = 0                |                       | 0                                         |                    | 6       | V    |
| V <sub>OD1</sub>  | Differential output voltage                                       | I <sub>O</sub> = 0                |                       | 1.5                                       |                    | 6       | V    |
| V <sub>OD2</sub>  | Differential output voltage                                       | R <sub>L</sub> = 100 Ω            | See Figure 6-1        | $\frac{1}{2} V_{OD1}$ or 2 <sup>(3)</sup> |                    |         | V    |
|                   |                                                                   | R <sub>L</sub> = 54 Ω             | See Figure 6-1        | 1.5                                       | 2.5                | 5       | V    |
| V <sub>OD3</sub>  | Differential output voltage                                       | V <sub>test</sub> = -7 V to 12 V, | See Figure 6-2        | 1.5                                       |                    | 5       | V    |
| Δ V <sub>OD</sub> | Change in magnitude of differential output voltage <sup>(4)</sup> | R <sub>L</sub> = 54 Ω or 100 Ω    | See Figure 6-1        |                                           |                    | ±0.2    | V    |
| V <sub>OC</sub>   | Common-mode output voltage                                        | R <sub>L</sub> = 54 Ω or 100 Ω    | See Figure 6-1        |                                           |                    | 3<br>-1 | V    |
| Δ V <sub>OC</sub> | Change in magnitude of common-mode output voltage <sup>(4)</sup>  | R <sub>L</sub> = 54 Ω or 100 Ω    | See Figure 6-1        |                                           |                    | ±0.2    | V    |
| I <sub>O</sub>    | Output current                                                    | Outputs disabled <sup>(6)</sup>   | V <sub>O</sub> = 12 V |                                           |                    | 1       | mA   |
|                   |                                                                   |                                   | V <sub>O</sub> = -7 V |                                           |                    | -0.8    |      |
| I <sub>IH</sub>   | High-level input current                                          | V <sub>I</sub> = 2.4 V            |                       |                                           |                    | 20      | μA   |
| I <sub>IL</sub>   | Low-level input current                                           | V <sub>I</sub> = 0.4 V            |                       |                                           |                    | -400    | μA   |
| I <sub>OS</sub>   | Short-circuit output current <sup>(5)</sup>                       | V <sub>O</sub> = -4 V             | SN65ALS176            |                                           |                    | -250    | mA   |
|                   |                                                                   | V <sub>O</sub> = -6 V             | SN75ALS176            |                                           |                    | -250    |      |
|                   |                                                                   | V <sub>O</sub> = 0                |                       |                                           |                    | -150    |      |
|                   |                                                                   | V <sub>O</sub> = V <sub>CC</sub>  |                       |                                           |                    | 250     |      |
|                   |                                                                   | V <sub>O</sub> = 8 V              |                       |                                           |                    | 250     |      |
| I <sub>CC</sub>   | Supply current                                                    | No load                           | Outputs enabled       |                                           | 23                 | 30      | mA   |
|                   |                                                                   |                                   | Outputs disabled      |                                           | 19                 | 26      |      |

- (1) The power-off measurement in TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.  
(2) All typical values are at V<sub>CC</sub> = 5 V and T<sub>A</sub> = 25°C.  
(3) The minimum V<sub>OD2</sub> with a 100-Ω load is either 1/2 V<sub>OD1</sub> or 2 V, whichever is greater.  
(4) Δ|V<sub>OD</sub>| and Δ|V<sub>OC</sub>| are the changes in magnitude of VOD and VOC, respectively, that occur when the input is changed from one logic state to the other.  
(5) Duration of the short circuit should not exceed one second for this test.  
(6) This applies for power on and power off. Refer to TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

## 5.5 Switching Characteristics - Driver

### SN65ALS176

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

| PARAMETER            |                                     | TEST CONDITIONS        |                         |                | MIN | TYP <sup>(1)</sup> | MAX | UNIT |
|----------------------|-------------------------------------|------------------------|-------------------------|----------------|-----|--------------------|-----|------|
| t <sub>d(OD)</sub>   | Differential output delay time      | R <sub>L</sub> = 54 Ω  | C <sub>L</sub> = 50 pF, | See Figure 6-3 |     |                    | 15  | ns   |
| t <sub>sk(p)</sub>   | Pulse skew <sup>(2)</sup>           | R <sub>L</sub> = 54 Ω  | C <sub>L</sub> = 50 pF, | See Figure 6-3 |     | 0                  | 2   | ns   |
| t <sub>sk(lim)</sub> | Pulse skew <sup>(3)</sup>           | R <sub>L</sub> = 54 Ω  | C <sub>L</sub> = 50 pF, | See Figure 6-3 |     |                    | 15  | ns   |
| t <sub>t(OD)</sub>   | Differential output transition time | R <sub>L</sub> = 54 Ω  | C <sub>L</sub> = 50 pF, | See Figure 6-3 |     | 8                  |     | ns   |
| t <sub>PZH</sub>     | Output enable time to high level    | R <sub>L</sub> = 110 Ω | C <sub>L</sub> = 50 pF, | See Figure 6-4 |     |                    | 80  | ns   |
| t <sub>PZL</sub>     | Output enable time to low level     | R <sub>L</sub> = 110 Ω | C <sub>L</sub> = 50 pF, | See Figure 6-5 |     |                    | 30  | ns   |
| t <sub>PHZ</sub>     | Output disable time from high level | R <sub>L</sub> = 110 Ω | C <sub>L</sub> = 50 pF, | See Figure 6-4 |     |                    | 50  | ns   |
| t <sub>PLZ</sub>     | Output disable time from low level  | R <sub>L</sub> = 110 Ω | C <sub>L</sub> = 50 pF, | See Figure 6-5 |     |                    | 30  | ns   |

- (1) All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

- (2) Pulse skew is defined as the  $|t_{PLH} - t_{PHL}|$  of each channel of the same device.  
(3) Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

## 5.6 Switching Characteristics - Driver

### SN75ALS176, SN75ALS176A, SN75ALS176B

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

| PARAMETER     |                                     |          | TEST CONDITIONS    |                       |                | MIN | TYP <sup>(1)</sup> | MAX  | UNIT |
|---------------|-------------------------------------|----------|--------------------|-----------------------|----------------|-----|--------------------|------|------|
| $t_{d(OD)}$   | Differential output delay time      | 'ALS176  | $R_L = 54 \Omega$  | $C_L = 50 \text{ pF}$ | See Figure 6-3 | 3   | 8                  | 13   | ns   |
|               |                                     | 'ALS176A |                    |                       |                | 4   | 7                  | 11.5 |      |
|               |                                     | 'ALS176B |                    |                       |                | 5   | 8                  | 10   |      |
| $t_{sk(p)}$   | Pulse skew <sup>(2)</sup>           |          | $R_L = 54 \Omega$  | $C_L = 50 \text{ pF}$ | See Figure 6-3 |     | 0                  | 2    | ns   |
| $t_{sk(lim)}$ | Pulse skew <sup>(3)</sup>           | 'ALS176  | $R_L = 54 \Omega$  | $C_L = 50 \text{ pF}$ | See Figure 6-3 |     |                    | 10   | ns   |
|               |                                     | 'ALS176A |                    |                       |                |     |                    | 7.5  |      |
|               |                                     | 'ALS176B |                    |                       |                |     |                    | 5    |      |
| $t_{i(OD)}$   | Differential output transition time |          | $R_L = 54 \Omega$  | $C_L = 50 \text{ pF}$ | See Figure 6-3 |     | 8                  |      | ns   |
| $t_{PZH}$     | Output enable time to high level    |          | $R_L = 110 \Omega$ | $C_L = 50 \text{ pF}$ | See Figure 6-4 |     | 23                 | 50   | ns   |
| $t_{PZL}$     | Output enable time to low level     |          | $R_L = 110 \Omega$ | $C_L = 50 \text{ pF}$ | See Figure 6-5 |     | 14                 | 20   | ns   |
| $t_{PHZ}$     | Output disable time from high level |          | $R_L = 110 \Omega$ | $C_L = 50 \text{ pF}$ | See Figure 6-4 |     | 20                 | 35   | ns   |
| $t_{PLZ}$     | Output disable time from low level  |          | $R_L = 110 \Omega$ | $C_L = 50 \text{ pF}$ | See Figure 6-5 |     | 8                  | 17   | ns   |

- (1) All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .  
(2) Pulse skew is defined as the  $|t_{PLH} - t_{PHL}|$  of each channel of the same device.  
(3) Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

## 5.7 Symbol Equivalents

| DATA-SHEET<br>PARAMETER | TIA/EIA-422-B           | TIA/EIA-485-A                             |
|-------------------------|-------------------------|-------------------------------------------|
| $V_O$                   | $V_{oa}, V_{ob}$        | $V_{oa}, V_{ob}$                          |
| $ V_{OD1} $             | $V_o$                   | $V_o$                                     |
| $ V_{OD2} $             | $V_t(R_L = 100 \Omega)$ | $V_t(R_L = 54 \Omega)$                    |
| $ V_{OD3} $             | None                    | $V_t$<br>(test termination measurement 2) |
| $\Delta V_{OD} $        | $  V_t  -  V_t  $       | $  V_t  -  V_t  $                         |
| $V_{OC}$                | $ V_{os} $              | $ V_{os} $                                |
| $\Delta V_{OC} $        | $ V_{os} - V_{os} $     | $ V_{os} - V_{os} $                       |
| $I_{OS}$                | $ I_{sa} ,  I_{sb} $    | None                                      |
| $I_O$                   | $ I_{xa} ,  I_{xb} $    | $I_{ia}, I_{ib}$                          |

## 5.8 Electrical Characteristics - Receiver

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature range (unless otherwise noted)

| PARAMETER |                                            | TEST CONDITIONS                              |                             | MIN                 | TYP <sup>(1)</sup> | MAX      | UNIT          |
|-----------|--------------------------------------------|----------------------------------------------|-----------------------------|---------------------|--------------------|----------|---------------|
| $V_{IT+}$ | Positive-going input threshold voltage     | $V_O = 2.7\text{ V}$ ,                       | $I_O = -0.4\text{ mA}$      |                     |                    | 0.2      | V             |
| $V_{IT-}$ | Negative-going input threshold voltage     | $V_O = 0.5\text{ V}$ ,                       | $I_O = 8\text{ mA}$         | -0.2 <sup>(2)</sup> |                    |          | V             |
| $V_{hys}$ | Hysteresis voltage ( $V_{IT+} - V_{IT-}$ ) |                                              |                             |                     | 60                 |          | mV            |
| $V_{IK}$  | Enable-input clamp voltage                 | $I_I = -18\text{ mA}$                        |                             |                     |                    | -1.5     | V             |
| $V_{OH}$  | High-level output voltage                  | $V_{ID} = 200\text{ mV}$ ,<br>See Figure 6-6 | $I_{OH} = -400\text{ mA}$ , | 2.7                 |                    |          | V             |
| $V_{OL}$  | Low-level output voltage                   | $V_{ID} = -200\text{ mV}$ ,<br>See Figure 6  | $I_{OL} = 8\text{ mA}$ ,    |                     |                    | 0.45     | V             |
| $I_{OZ}$  | High-impedance-state output current        | $V_O = 0.4\text{ V to } 2.4\text{ V}$        |                             |                     |                    | $\pm 20$ | $\mu\text{A}$ |
| $V_I$     | Line input current                         | Other input = 0 V <sup>(3)</sup>             | $V_I = 12\text{ V}$         |                     |                    | 1        | mA            |
|           |                                            |                                              | $V_I = -7\text{ V}$         |                     |                    | -0.8     |               |
| $I_{IH}$  | High-level-enable input current            | $V_{IH} = 2.7\text{ V}$                      |                             |                     |                    | 20       | $\mu\text{A}$ |
| $I_{IL}$  | Low-level-enable input current             | $V_{IL} = 0.4\text{ V}$                      |                             |                     |                    | -100     | $\mu\text{A}$ |
| $r_I$     | Input resistance                           |                                              |                             | 12                  | 20                 |          | k $\Omega$    |
| $I_{OS}$  | Short-circuit output current               | $V_{ID} = 200\text{ mV}$ ,                   | $V_O = 0$                   | -15                 |                    | -85      | mA            |
| $I_{CC}$  | Supply current                             | No load                                      | Outputs enabled             |                     | 23                 | 30       | mA            |
|           |                                            |                                              | Outputs disabled            |                     | 19                 | 26       |               |

(1) All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

(2) The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

(3) This applies for power on and power off. Refer to TIA/EIA-485-A for exact conditions.

## 5.9 Switching Characteristics - Receiver

### SN65ALS176

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

| PARAMETER     |                                     | TEST CONDITIONS                                               |                        | MIN | TYP <sup>(1)</sup> | MAX | UNIT |
|---------------|-------------------------------------|---------------------------------------------------------------|------------------------|-----|--------------------|-----|------|
| $t_{pd}$      | Propagation time                    | $V_{ID} = -1.5\text{ V to } 1.5\text{ V}$ ,<br>See Figure 6-7 | $C_L = 15\text{ pF}$ , |     |                    | 25  | ns   |
| $t_{sk(p)}$   | Pulse skew <sup>(2)</sup>           | $V_{ID} = -1.5\text{ V to } 1.5\text{ V}$ ,<br>See Figure 6-7 | $C_L = 15\text{ pF}$ , |     | 0                  | 2   | ns   |
| $t_{sk(lim)}$ | Pulse skew <sup>(3)</sup>           | $R_L = 54\text{ }\Omega$<br>See Figure 6-3                    | $C_L = 50\text{ pF}$ , |     |                    | 15  | ns   |
| $t_{PZH}$     | Output enable time to high level    | $C_L = 15\text{ pF}$ ,                                        | See Figure 6-8         |     | 11                 | 18  | ns   |
| $t_{PZL}$     | Output enable time to low level     | $C_L = 15\text{ pF}$ ,                                        | See Figure 6-8         |     | 11                 | 18  | ns   |
| $t_{PHZ}$     | Output disable time from high level | $C_L = 15\text{ pF}$ ,                                        | See Figure 6-8         |     |                    | 50  | ns   |
| $t_{PLZ}$     | Output disable time from low level  | $C_L = 15\text{ pF}$ ,                                        | See Figure 6-8         |     |                    | 30  | ns   |

(1) All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

(2) Pulse skew is defined as the  $|t_{PLH} - t_{PHL}|$  of each channel of the same device.

(3) Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

## 5.10 Switching Characteristics - Receiver

### SN75ALS176, SN75ALS176A, SN75ALS176B

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

| PARAMETER     |                                     |          | TEST CONDITIONS                                                              |                                | MIN  | TYP <sup>(1)</sup> | MAX  | UNIT |
|---------------|-------------------------------------|----------|------------------------------------------------------------------------------|--------------------------------|------|--------------------|------|------|
| $t_{pd}$      | Propagation time                    | 'ALS176  | $V_{ID} = -1.5\text{ V to }1.5\text{ V}$ ,<br>See <a href="#">Figure 6-7</a> | $C_L = 15\text{ pF}$ ,         | 9    | 14                 | 19   | ns   |
|               |                                     | 'ALS176A |                                                                              |                                | 10.5 | 14                 | 18   |      |
|               |                                     | 'ALS176B |                                                                              |                                | 11.5 | 13                 | 16.5 |      |
| $t_{sk(p)}$   | Pulse skew <sup>(2)</sup>           |          | $V_{ID} = -1.5\text{ V to }1.5\text{ V}$ ,<br>See <a href="#">Figure 6-7</a> | $C_L = 15\text{ pF}$ ,         |      | 0                  | 2    | ns   |
| $t_{sk(lim)}$ | Pulse skew <sup>(3)</sup>           | 'ALS176  | $R_L = 54\ \Omega$<br>See <a href="#">Figure 6-3</a>                         | $C_L = 50\text{ pF}$ ,         |      |                    | 10   | ns   |
|               |                                     | 'ALS176A |                                                                              |                                |      |                    | 7.5  |      |
|               |                                     | 'ALS176B |                                                                              |                                |      |                    | 5    |      |
| $t_{PZH}$     | Output enable time to high level    |          | $C_L = 15\text{ pF}$ ,                                                       | See <a href="#">Figure 6-8</a> |      | 7                  | 14   | ns   |
| $t_{PZL}$     | Output enable time to low level     |          | $C_L = 15\text{ pF}$ ,                                                       | See <a href="#">Figure 6-8</a> |      | 20                 | 35   | ns   |
| $t_{PHZ}$     | Output disable time from high level |          | $C_L = 15\text{ pF}$ ,                                                       | See <a href="#">Figure 6-8</a> |      | 20                 | 35   | ns   |
| $t_{PLZ}$     | Output disable time from low level  |          | $C_L = 15\text{ pF}$ ,                                                       | See <a href="#">Figure 6-8</a> |      | 8                  | 17   | ns   |

(1) All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

(2) Pulse skew is defined as the  $|t_{PLH} - t_{PHL}|$  of each channel of the same device.

(3) Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

## 5.11 Typical Characteristics

Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

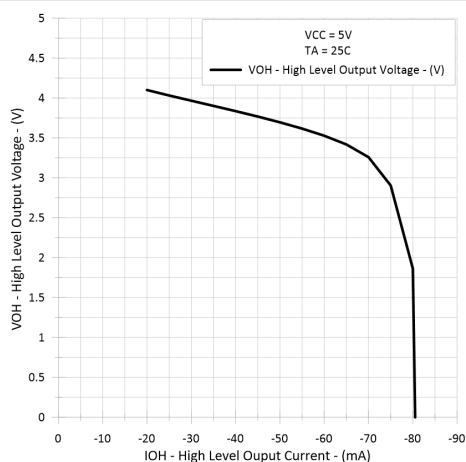


**Figure 5-1. Driver High-Level Output Voltage vs High-Level Output Current**

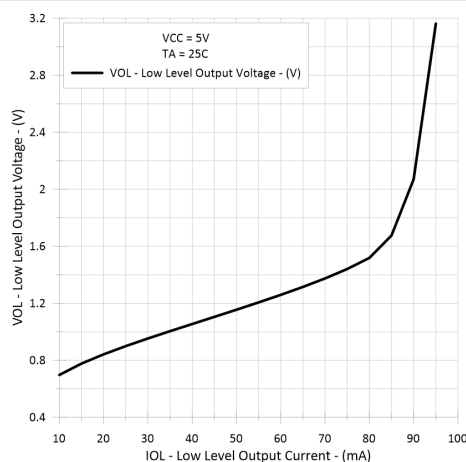


**Figure 5-2. Driver Low-Level Output Voltage vs Low-Level Output Current**

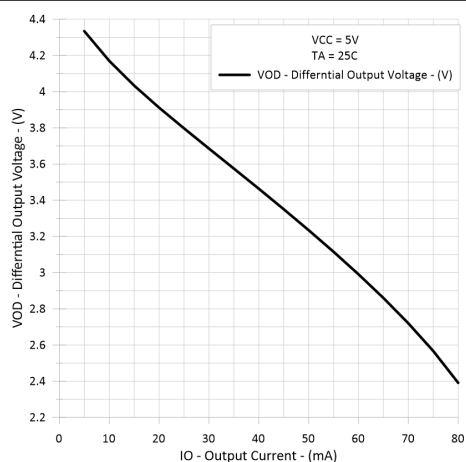


**Figure 5-3. Driver Differential Output Voltage vs Output Current**

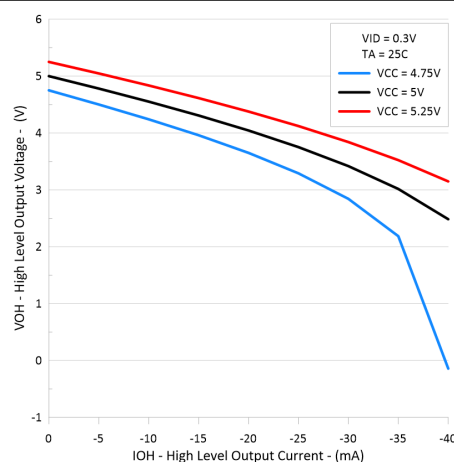


**Figure 5-4. Receiver High-Level Output Voltage vs High-Level Output Current**

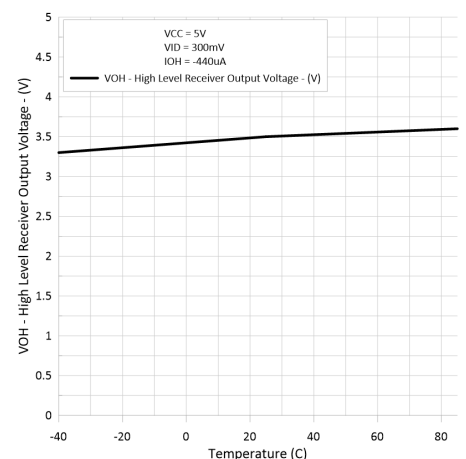


**Figure 5-5. Receiver High-Level Output Voltage vs Free-Air Temperature**

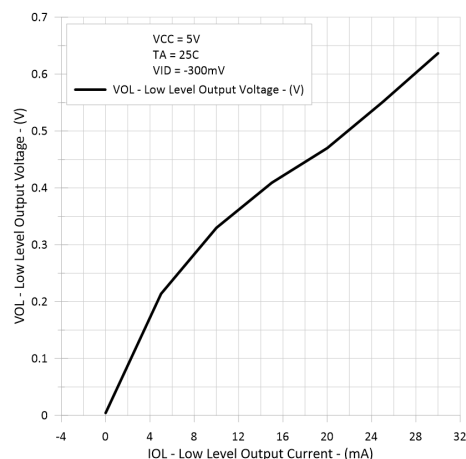


**Figure 5-6. Receiver Low-Level Output Voltage vs Low-Level Output Current**

## 5.11 Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

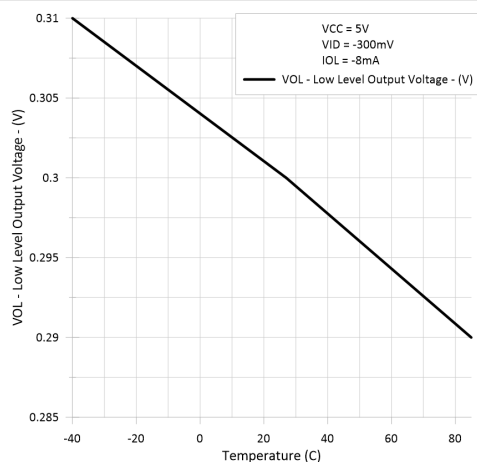


**Figure 5-7. Receiver Low-Level Output Voltage vs Free-Air Temperature**

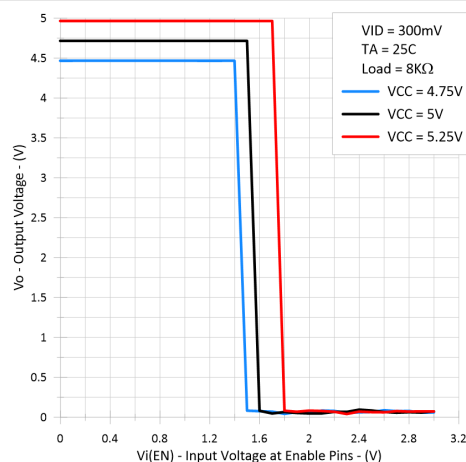


**Figure 5-8. Receiver Output Voltage vs Enable Voltage**

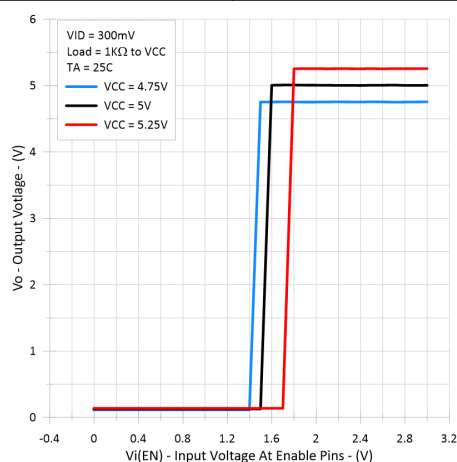


**Figure 5-9. Receiver Output Voltage vs Enable Voltage**

## 6 Parameter Measurement Information

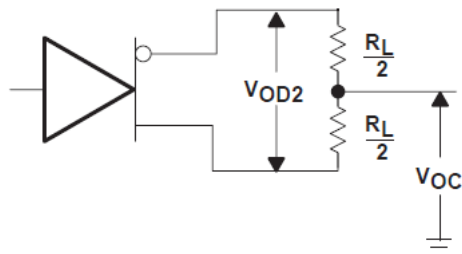


Figure 6-1. Driver  $V_{OD2}$  and  $V_{OC}$

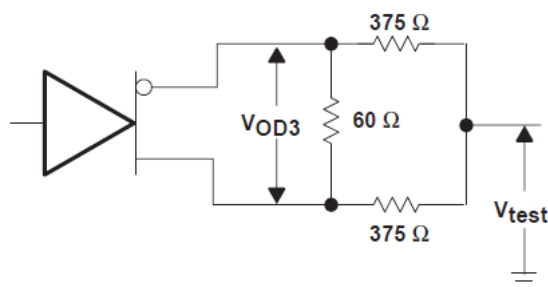
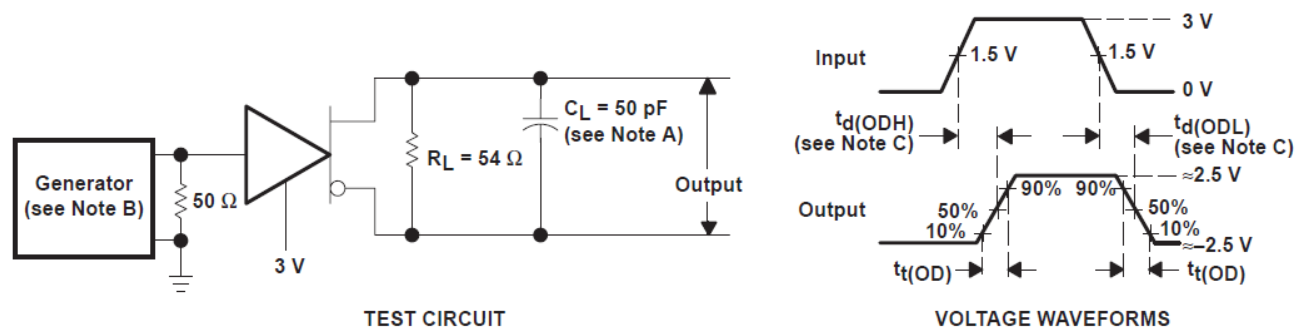
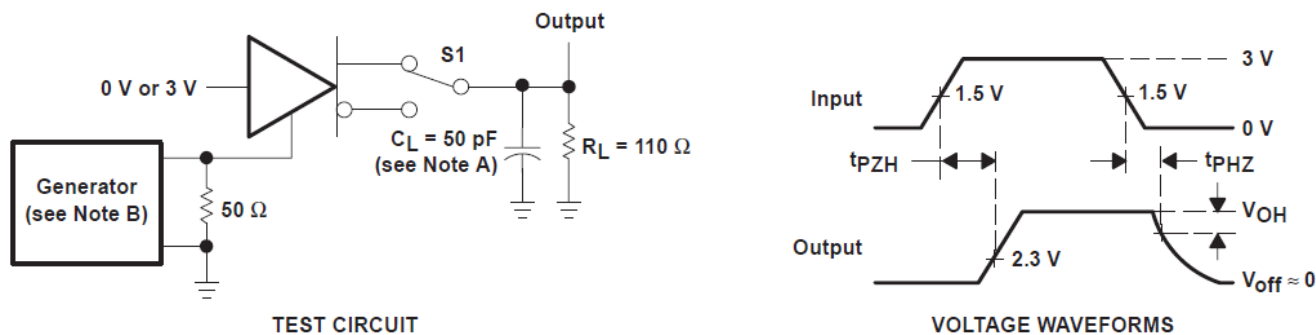


Figure 6-2. Driver  $V_{OD3}$



- A.  $C_L$  includes probe and jig capacitance.  
B. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq 1$  MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .

Figure 6-3. Driver Test Circuit and Voltage Waveforms



- A.  $C_L$  includes probe and jig capacitance.

- B. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1$  MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .

**Figure 6-4. Driver Test Circuit and Voltage Waveforms**

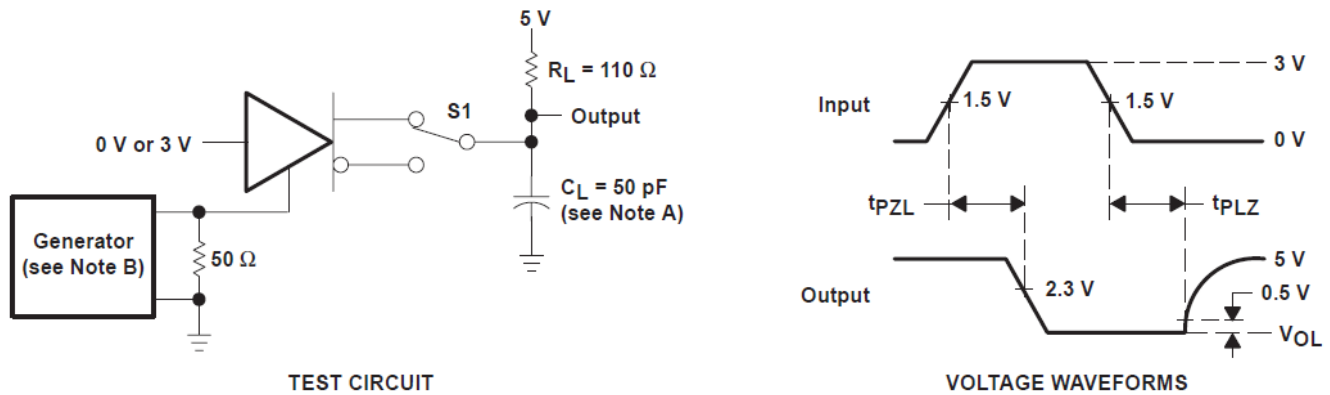


**Figure 6-5. Driver Test Circuit and Voltage Waveforms**

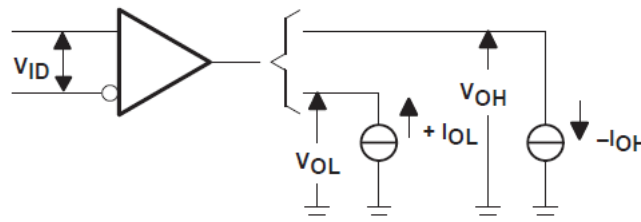
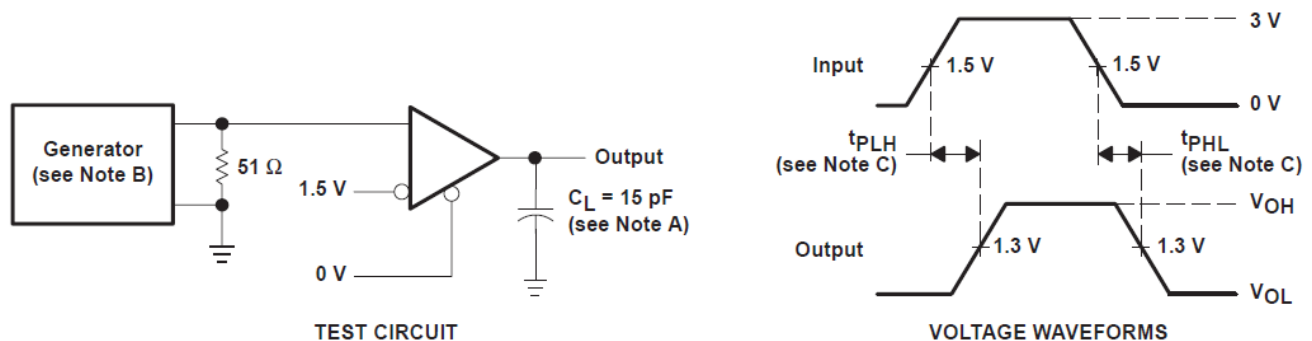
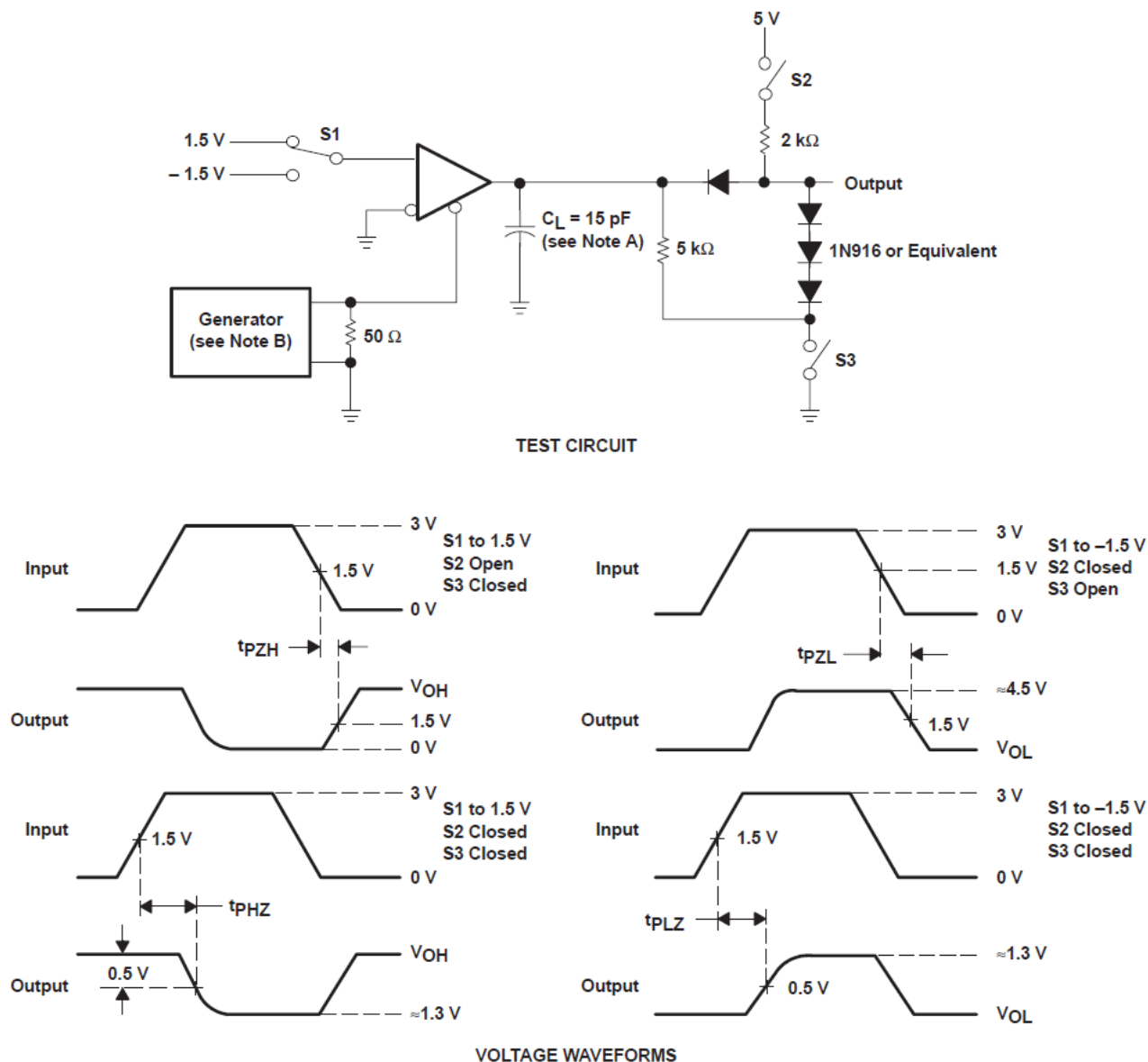


**Figure 6-6. Receiver  $V_{OH}$  and  $V_{OL}$  Test Circuit**



- A.  $C_L$  includes probe and jig capacitance.  
 B. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1$  MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .  
 C.  $t_{pd} = t_{PLH}$  or  $t_{PHL}$ .

**Figure 6-7. Receiver Test Circuit and Voltage Waveforms**



- A.  $C_L$  includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, 50% duty cycle,  $t_r \leq$  6 ns,  $t_f \leq$  6 ns,  $Z_O = 50 \Omega$ .

**Figure 6-8. Receiver Test Circuit and Voltage Waveforms**

## 7 Detailed Description

### 7.1 Functional Block Diagram

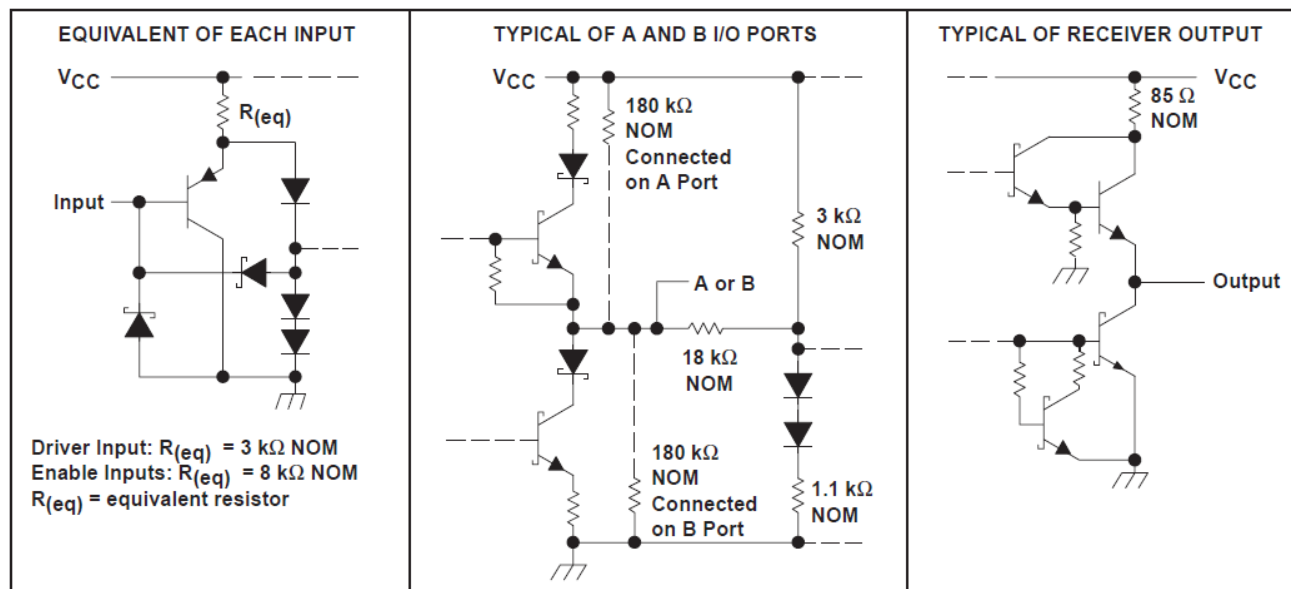


Figure 7-1. Schematic of Inputs and Outputs

### 7.2 Device Functional Modes

#### Function Tables

Table 7-1. Driver<sup>(1)</sup>

| INPUT<br>D | ENABLE<br>DE | OUTPUTS |   |
|------------|--------------|---------|---|
|            |              | A       | B |
| H          | H            | H       | L |
| L          | H            | L       | H |
| X          | L            | Z       | Z |

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

Table 7-2. Receiver<sup>(1)</sup>

| DIFFERENTIAL INPUTS<br>A-B                | ENABLE<br>RE | OUTPUT<br>R |
|-------------------------------------------|--------------|-------------|
| $V_{ID} \geq 0.2 \text{ V}$               | L            | H           |
| $-0.2 \text{ V} < V_{ID} < 0.2 \text{ V}$ | L            | ?           |
| $V_{ID} \leq -0.2 \text{ V}$              | L            | L           |
| X                                         | H            | Z           |
| Inputs open                               | L            | H           |

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

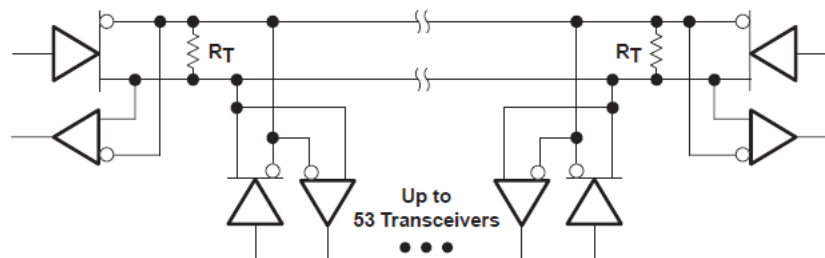
## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

### 8.2 Typical Application



- A. The line should terminate at both ends in its characteristic impedance ( $R_T = Z_0$ ). Stub lengths off the main line should be kept as short as possible.

**Figure 8-1. Typical Application Circuit**

## 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number         | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN65ALS176DR</a>  | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 65A176              |
| SN65ALS176DR.A                | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 65A176              |
| SN65ALS176DR1G4               | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 65A176              |
| SN65ALS176DR1G4.A             | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | 65A176              |
| <a href="#">SN75ALS176AD</a>  | Active        | Production           | SOIC (D)   8   | 75   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 7A176A              |
| SN75ALS176AD.A                | Active        | Production           | SOIC (D)   8   | 75   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 7A176A              |
| <a href="#">SN75ALS176ADR</a> | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 7A176A              |
| SN75ALS176ADR.A               | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 7A176A              |
| SN75ALS176ADRG4               | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 7A176A              |
| <a href="#">SN75ALS176AP</a>  | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | 75ALS176A           |
| SN75ALS176AP.A                | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | 75ALS176A           |
| <a href="#">SN75ALS176BD</a>  | Obsolete      | Production           | SOIC (D)   8   | -                     | -           | Call TI                              | Call TI                           | 0 to 70      | 7A176B              |
| <a href="#">SN75ALS176BDR</a> | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | (75A176, 7A176B)    |
| SN75ALS176BDR.A               | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | (75A176, 7A176B)    |
| <a href="#">SN75ALS176BP</a>  | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | 75ALS176B           |
| SN75ALS176BP.A                | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | 75ALS176B           |
| <a href="#">SN75ALS176D</a>   | Obsolete      | Production           | SOIC (D)   8   | -                     | -           | Call TI                              | Call TI                           | 0 to 70      | 75A176              |
| <a href="#">SN75ALS176P</a>   | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | 75ALS176            |
| SN75ALS176P.A                 | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | 75ALS176            |
| SN75ALS176PE4                 | Active        | Production           | PDIP (P)   8   | 50   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | 75ALS176            |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

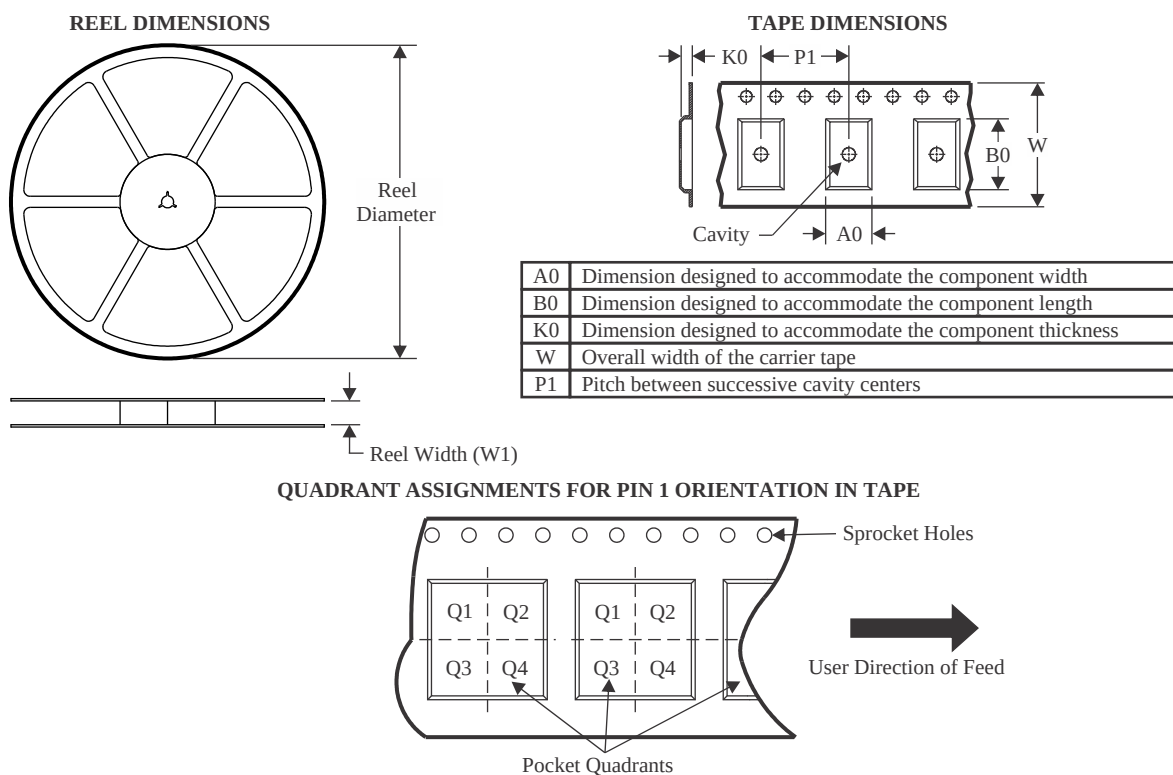
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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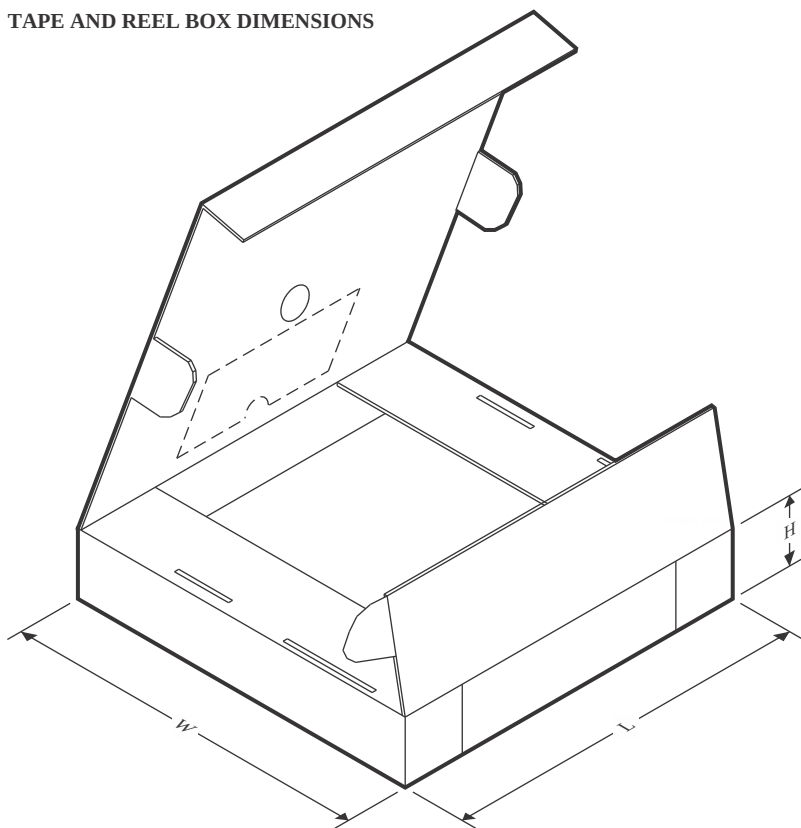
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65ALS176DR    | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| SN65ALS176DR1G4 | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| SN75ALS176ADR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| SN75ALS176BDR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |

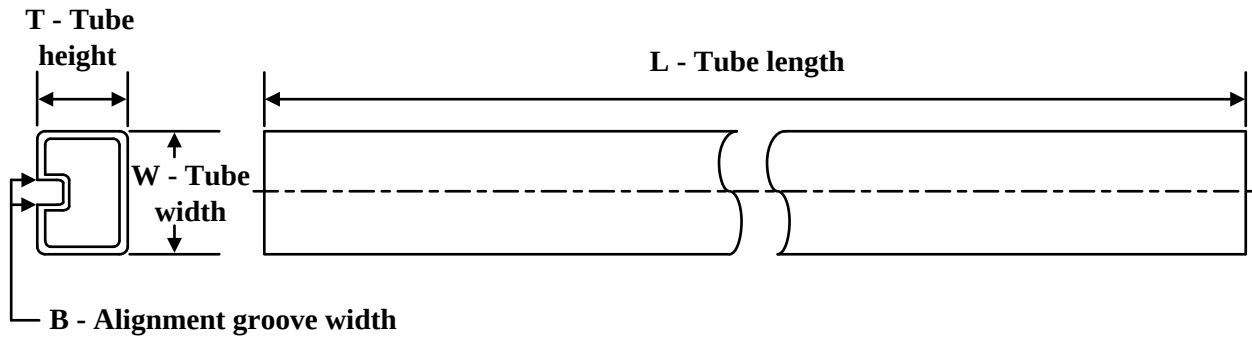
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65ALS176DR    | SOIC         | D               | 8    | 2500 | 340.5       | 336.1      | 25.0        |
| SN65ALS176DR1G4 | SOIC         | D               | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| SN75ALS176ADR   | SOIC         | D               | 8    | 2500 | 353.0       | 353.0      | 32.0        |
| SN75ALS176BDR   | SOIC         | D               | 8    | 2500 | 340.5       | 336.1      | 25.0        |

## TUBE



\*All dimensions are nominal

| Device         | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN75ALS176AD   | D            | SOIC         | 8    | 75  | 507    | 8      | 3940   | 4.32   |
| SN75ALS176AD.A | D            | SOIC         | 8    | 75  | 507    | 8      | 3940   | 4.32   |
| SN75ALS176AP   | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| SN75ALS176AP.A | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| SN75ALS176BP   | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| SN75ALS176BP.A | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| SN75ALS176P    | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| SN75ALS176P.A  | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| SN75ALS176PE4  | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |



## PACKAGE OUTLINE

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



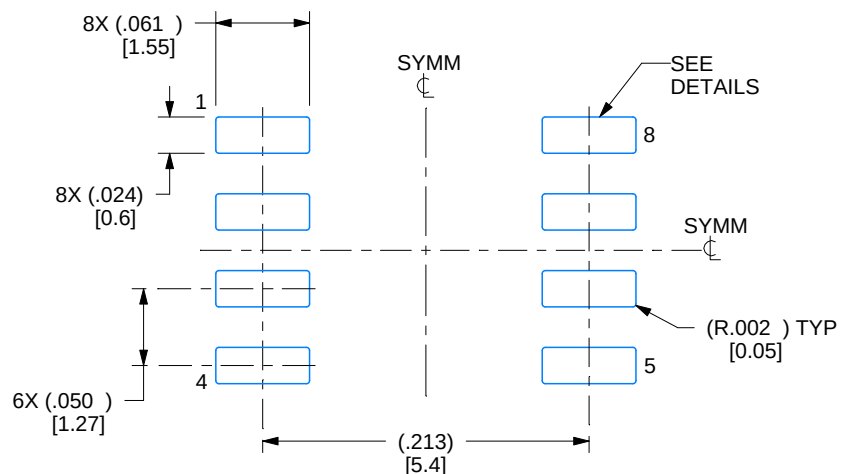
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

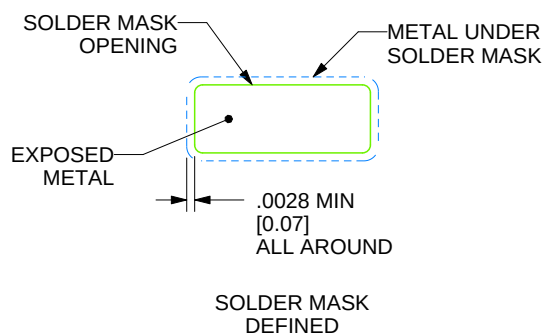
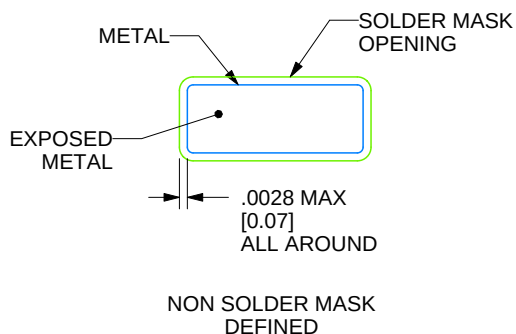
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

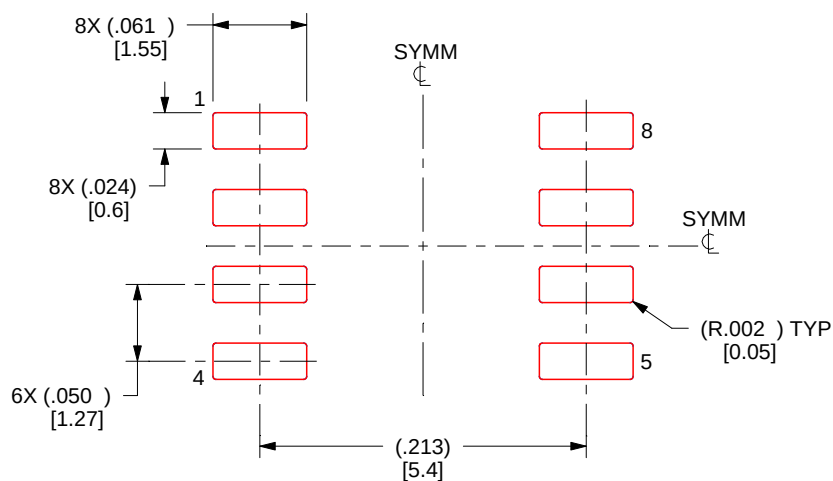
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

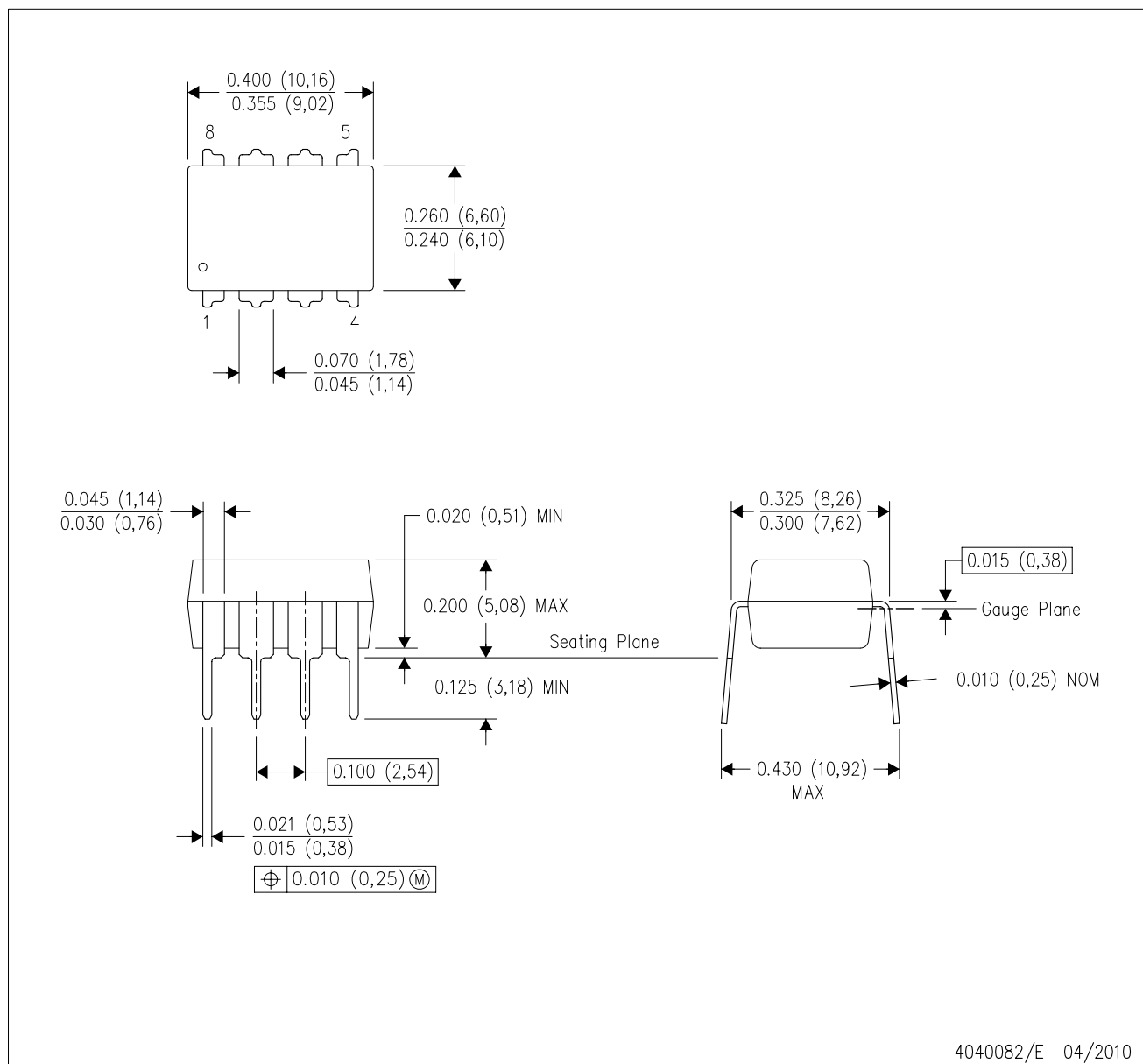
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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

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