TEXAS INSTRUMENTS

SN65HVD1780, SN65HVD1781, SN65HVD1782

SLLS877H – DECEMBER 2007 – REVISED MARCH 2017

SN65HVD178x Fault-Protected RS-485 Transceivers With 3.3-V to 5-V Operation

1 Features

- Bus-Pin Fault Protection to:
  - > ±70 V (SN65HVD1780, SN65HVD1781)
  - > ±30 V (SN65HVD1782)
- Operation With 3.3-V to 5-V Supply Range
- ±16-kV HBM Protection on Bus Pins
- Reduced Unit Load for Up to 320 Nodes
- Failsafe Receiver for Open-Circuit, Short-Circuit, and Idle-Bus Conditions
- Low Power Consumption
  - Low Standby Supply Current, 1 µA Maximum
  - I_{CC} 4-mA Quiescent Current During Operation
- Pin-Compatible With Industry-Standard SN75176
- Signaling Rates of 115 kbps, 1 Mbps, and up to 10 Mbps
- Create a Custom Design using the SN65HVD178x with the WEBENCH® Power Designer

2 Applications

- HVAC Networks
- Security Electronics
- Building Automation
- Telecommunication Equipment
- Motion Control
- Industrial Networks

3 Description

The SN65HVD178x devices are designed to survive overvoltage faults such as direct shorts to power supplies, mis-wiring faults, connector failures, cable crushes, and tool mis-applications. The devices are also robust to ESD events with high levels of protection to the human-body-model specification.

The SN65HVD178x devices combine a differential driver and a differential receiver, which operate from a single power supply. In the SN65HVD1782, the driver differential outputs and the receiver differential inputs are connected internally to form a bus port suitable for half-duplex (two-wire bus) communication. This port features a wide common-mode voltage range, making the devices suitable for multipoint applications over long cable runs. These devices are characterized from –40°C to 125°C. These devices are pin-compatible with the industry-standard SN75176 transceiver, making them drop-in upgrades in most systems.

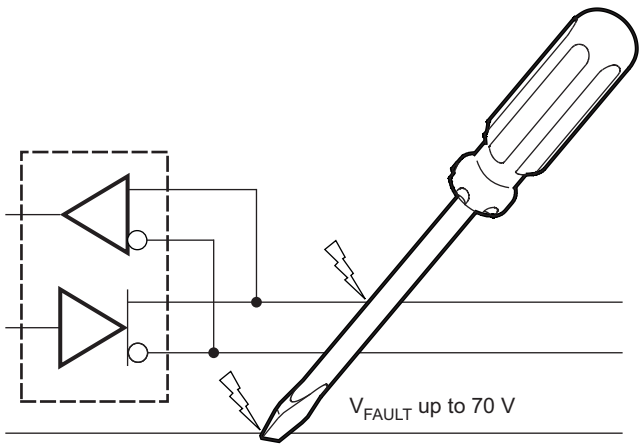
These devices are fully compliant with ANSI TIA/EIA 485-A with a 5-V supply and can operate with a 3.3-V supply with reduced driver output voltage for low-power applications. For applications where operation is required over an extended common-mode voltage range, see the SN65HVD1785 (SLLS872) data sheet.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65HVD178x	SOIC (8)	4.90 mm × 3.91 mm
	PDIP (8)	9.81 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Protection Against Bus Shorts



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (August 2015) to Revision H — **Page**

- Added WEBENCH information to the *Features*, *Detailed Design Procedure*, and *Device Support* sections ... 1
- Added values to the Storage temperature in the *Absolute Maximum Ratings* table ... 4
- Added the *Equivalent Input Schematic* section ... 14

Changes from Revision F (August 2012) to Revision G — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision E (September 2008) to Revision F — **Page**

- Deleted text from the first Description paragraph - The internal current-limit circuits allow fault survivability without causing the high bus currents that otherwise might damage external components or power supplies. ... 1
- Changed From: Voltage input range, transient pulse, A and B, through 100 Ω in the *Absolute Maximum Ratings* table To: Transient overvoltage pulse through 100 Ω per TIA-485 ... 4
- Changed Figure 13 title From: Measurement of Receiver Enable Times With Driver Disabled To: Measurement of Receiver Enable Times With Driver Disabled ... 13

Changes from Revision D (August 2008) to Revision E — **Page**

- Changed Bus input current (disabled driver), separating the condition for the different devices. ... 6

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Changes from Revision C (July 2008) to Revision D **Page**

- Changed Receiver propagation delay max value From: 70 ns To: 80 ns. ... 8

Changes from Revision B (April 2008) to Revision C **Page**

- Added two new part numbers 1780 and 1782 ... 1
- Deleted Features Bullet: Designed for RS-485 and RS-422 Networks ... 1
- Changed making it a drop-in upgrade for most devices -to- making them drop-in upgrades in most systems. ... 1

Changes from Revision A (January 2008) to Revision B **Page**

- Changed the I_{OS} Min value From: -150 To: -200 and Max value From: 150 To: 200 ... 6

Changes from Original (December 2007) to Revision A **Page**

- Changed Receiver propagation delay max value From: 50 ns To: 70 ns. ... 8
- Changed t_{PLZ}, t_{PHZ} Receiver disable time From 3000 ns To 100 ns. ... 8

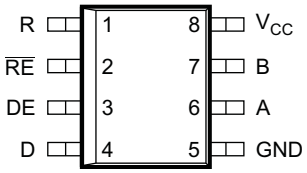
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5 Device Comparison Table

TRANSCEIVER	SIGNALING RATE	NUMBER OF NODES
SN65HVD1780	Up to 115 kbps	Up to 320
SN65HVD1781	Up to 1 Mbps	Up to 320
SN65HVD1782	Up to 10 Mbps	Up to 64

6 Pin Configuration and Functions

D Package and P Package
8-Pin SOIC and 8-Pin PDIP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
A	6	Bus input/output	Driver output or receiver input (complimentary to B)
B	7	Bus input/output	Driver output or receiver input (complimentary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable high
GND	5	Reference potential	Local device ground
R	1	Digital output	Receive data output
$\overline{RE}$	2	Digital input	Receiver enable low
V_{CC}	8	Supply	4.5-V to 5.5-V supply

7 Specifications

7.1 Absolute Maximum Ratings(1)

			MIN	MAX	UNIT
Supply voltage, V_{CC}			–0.5	7	V
Voltage at bus pin	SN65HVD1780, SN65HVD1781	A, B pins	–70	70	V
	SN65HVD1782	A, B pins	–70	30	
Input voltage at any logic pin			–0.3	V_{CC} + 0.3	V
Transient overvoltage pulse through 100 Ω per TIA-485			–70	70	V
Receiver output current			–24	24	mA
Junction temperature, T_J				170	°C
Storage temperature, T_{stg}			–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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7.2 ESD Ratings: JEDEC

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	Bus pins and GND	±16000	V
			All pins	±4000	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)		±2000	
		Machine model JEDEC Standard 22, Test Method A115, all pins		±400	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 ESD Ratings: IEC

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 60749-26 ESD (human body model), bus terminals and GND	±16000	V

7.4 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3.15	5	5.5	V
V_I	Input voltage at any bus terminal (separately or common mode)(1)		–7		12	V
V_{IH}	High-level input voltage (driver, driver enable, and receiver enable inputs)		2		V_{CC}	V
V_{IL}	Low-level input voltage (driver, driver enable, and receiver enable inputs)		0		0.8	V
V_{ID}	Differential input voltage		–12		12	V
I_O	Output current, driver		–60		60	mA
	Output current, receiver		–8		8	mA
R_L	Differential load resistance		54	60		Ω
C_L	Differential load capacitance			50		pF
$1/t_{UI}$	Signaling rate	SN65HVD1780			115	kbps
		SN65HVD1781			1	Mbps
		SN65HVD1782			10	
T_A	Operating free-air temperature (See *Power Dissipation Characteristics*)	5-V supply	–40		105	°C
		3.3-V supply	–40		125	
T_J	Junction temperature		–40		150	°C

(1) By convention, the least positive (most negative) limit is designated as minimum in this data sheet.

7.5 Thermal Information

THERMAL METRIC(1)			SN65HVD178x		UNIT
			D (SOIC)	P (PDIP)	
			8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	JEDEC high-K model	138	59	°C/W
		JEDEC low-K model	242	128	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		61	61	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		62	39	°C/W
ψ_{JT}	Junction-to-top characterization parameter		3.4	17.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter		33.4	28.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Driver differential output voltage magnitude	R_L = 60 Ω, 4.75 V ≤ V_{CC} 375 Ω on each output to –7 V to 12 V Figure 6		T_A < 85°C	1.5			V
				T_A < 125°C	1.4			
		R_L = 54 Ω, 4.75 V ≤ V_{CC} ≤ 5.25 V		T_A < 85°C	1.7	2		
				T_A < 125°C	1.5			
		R_L = 54 Ω, 3.15 V ≤ V_{CC} ≤ 3.45 V			0.8	1		
		R_L = 100 Ω, 4.75 V ≤ V_{CC} ≤ 5.25 V		T_A < 85°C	2.2	2.5		
				T_A < 125°C	2			
$\Delta\|V_{OD}\|$	Change in magnitude of driver differential output voltage	R_L = 54 Ω			–50	0	50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage				1	V_{CC}/2	3	V
ΔV_{OC}	Change in differential driver output common-mode voltage				–50	0	50	mV
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage	Center of two 27-Ω load resistors See Figure 7				500		mV
C_{OD}	Differential output capacitance					23		pF
V_{IT+}	Positive-going receiver differential input voltage threshold					–100	–35	mV
$V_{IT–}$	Negative-going receiver differential input voltage threshold				–180	–150		mV
V_{HYS}	Receiver differential input voltage threshold hysteresis ($V_{IT+} – V_{IT–}$)				30	50		mV
V_{OH}	Receiver high-level output voltage	I_{OH} = –8 mA			2.4	V_{CC} – 0.3		V
V_{OL}	Receiver low-level output voltage	I_{OL} = 8 mA		T_A < 85°C		0.2	0.4	V
				T_A < 125°C			0.5	
$I_{I(LOGIC)}$	Driver input, driver enable, and receiver enable input current				–50		50	µA
I_{OZ}	Receiver output high-impedance current	V_O = 0 V or V_{CC}, $\overline{RE}$ at V_{CC}			–1		1	µA
I_{OS}	Driver short-circuit output current				–200		200	mA
$I_{I(BUS)}$	Bus input current (disabled driver)	V_{CC} = 3.15 to 5.5 V or V_{CC} = 0 V, DE at 0 V	V_I = 12 V	1780, 1781		75	100	µA
				1782		400	500	
			V_I = –7 V	1780, 1781	–60	–40		
				1782	–400	–300		
I_{CC}	Supply current (quiescent)	Driver and receiver enabled		DE = V_{CC}, RE = GND, no load		4	6	mA
		Driver enabled, receiver disabled		DE = V_{CC}, RE = V_{CC}, no load		3	5	
		Driver disabled, receiver enabled		DE = GND, RE = GND, no load		2	4	
		Drive and receiver disabled (standby mode)		DE = GND, D = open, RE = V_{CC}, no load, T_A < 85°C		0.15	1	µA
				DE = GND, D = open, RE = V_{CC}, no load, T_A < 125°C			12	
	Supply current (dynamic)	See *Typical Characteristics*						

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7.7 Power Dissipation Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MAX	UNIT
P_D	Power dissipation	V_{CC} = 5.5 V, T_J = 150°C, R_L = 300 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 5-V supply, unterminated (1)	290	mW
		V_{CC} = 5.5 V, T_J = 150°C, R_L = 100 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 5-V supply, RS-422 load (1)	320	
		V_{CC} = 5.5 V, T_J = 150°C, R_L = 54 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 5-V supply, RS-485 load (1)	400	
T_{SD}	Thermal-shutdown junction temperature		170	°C

(1) Driver and receiver enabled, 50% duty cycle square-wave signal at signaling rate: 1 Mbps.

7.8 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER (SN65HVD1780)							
t_r, t_f	Driver differential output rise or fall time	R_L = 54 Ω, C_L = 50 pF, See Figure 8	3.15 V < V_{CC} < 3.45 V	0.4	1.4	1.8	µs
			3.15 V < V_{CC} < 5.5 V	0.4	1.7	2.6	
t_{PHL}, t_{PLH}	Driver propagation delay	R_L = 54 Ω, C_L = 50 pF, See Figure 8			0.8	2	µs
$t_{SK(P)}$	Driver differential output pulse skew, $\|t_{PHL} - t_{PLH}\|$	R_L = 54 Ω, C_L = 50 pF, See Figure 8			20	250	ns
t_{PHZ}, t_{PLZ}	Driver disable time	See Figure 9 and Figure 10			0.1	5	µs
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled	See Figure 9 and Figure 10		0.2	3	µs
		Receiver disabled	See Figure 9 and Figure 10		3	12	
DRIVER (SN65HVD1781)							
t_r, t_f	Driver differential output rise or fall time	R_L = 54 Ω, C_L = 50 pF, See Figure 8		50		300	ns
t_{PHL}, t_{PLH}	Driver propagation delay	R_L = 54 Ω, C_L = 50 pF, See Figure 8				200	ns
$t_{SK(P)}$	Driver differential output pulse skew, $\|t_{PHL} - t_{PLH}\|$	R_L = 54 Ω, C_L = 50 pF, See Figure 8				25	ns
t_{PHZ}, t_{PLZ}	Driver disable time	See Figure 9 and Figure 10				3	µs
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled	See Figure 9 and Figure 10			300	ns
		Receiver disabled	See Figure 9 and Figure 10			10	µs
DRIVER (SN65HVD1782)							
t_r, t_f	Driver differential output rise or fall time	R_L = 54 Ω, C_L = 50 pF	All V_{CC} and Temperature			50	ns
			V_{CC} > 4.5 V and T < 105°C		16		
t_{PHL}, t_{PLH}	Driver propagation delay	R_L = 54 Ω, C_L = 50 pF	See Figure 8			55	ns
$t_{SK(P)}$	Driver differential output pulse skew, $\|t_{PHL} - t_{PLH}\|$	R_L = 54 Ω, C_L = 50 pF	See Figure 8			10	ns
t_{PHZ}, t_{PLZ}	Driver disable time	See Figure 9 and Figure 10				3	µs

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Switching Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled	See Figure 9 and Figure 10			300	ns
		Receiver disabled	See Figure 9 and Figure 10			9	µs
RECEIVER							
t_r, t_f	Receiver output rise or fall time	C_L = 15 pF, See Figure 11	All devices		4	15	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time	C_L = 15 pF, See Figure 11	SN65HVD1780, SN65HVD1781		100	200	ns
			SN65HVD1782			80	
$t_{SK(P)}$	Receiver output pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$	C_L = 15 pF, See Figure 11	SN65HVD1780, SN65HVD1781		6	20	ns
			SN65HVD1782			5	
t_{PLZ}, t_{PHZ}	Receiver disable time	Driver enabled, See Figure 12			15	100	ns
$t_{PZL(1)}$, $t_{PZH(1)}$ $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time	Driver enabled, See Figure 12			80	300	ns
		Driver disabled, See Figure 13			3	9	µs

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7.9 Typical Characteristics

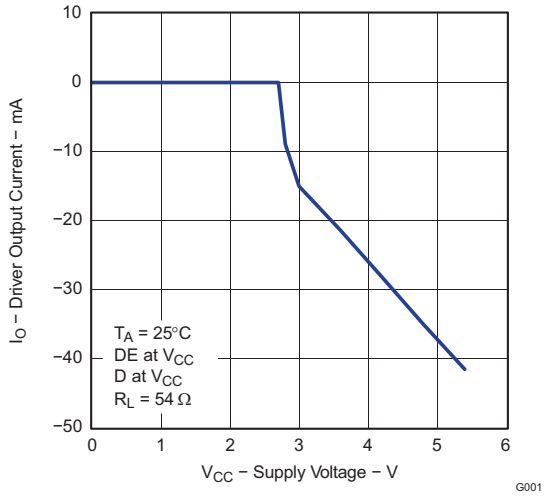


Figure 1. Driver Output Current vs Supply Voltage

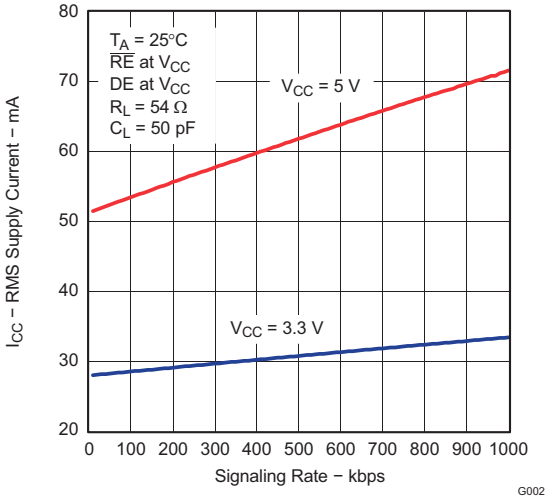


Figure 2. RMS Supply Current vs Signaling Rate

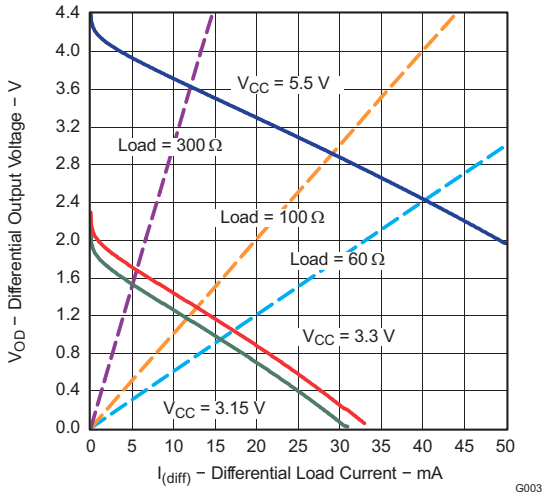


Figure 3. Differential Output Voltage vs Differential Load Current

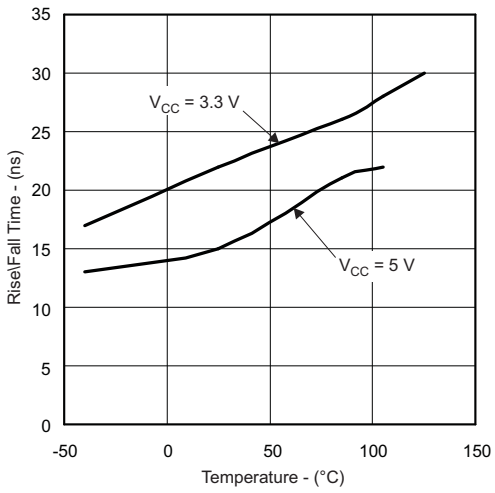


Figure 4. SN65HVD1782 Rise or Fall Time

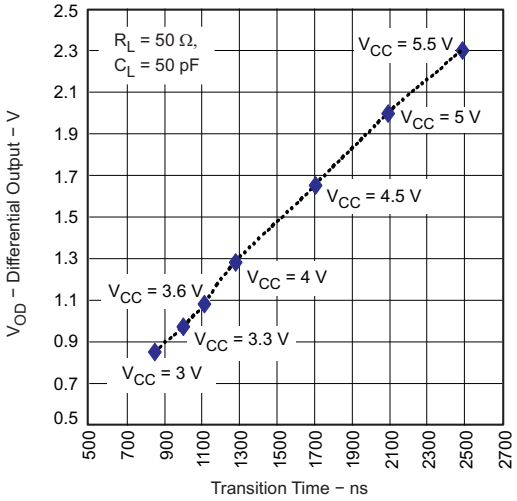
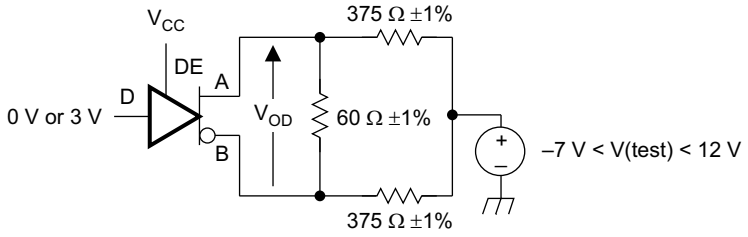


Figure 5. SN65HVD1780 Differential Output Amplitude and Transition Time vs Supply Voltage

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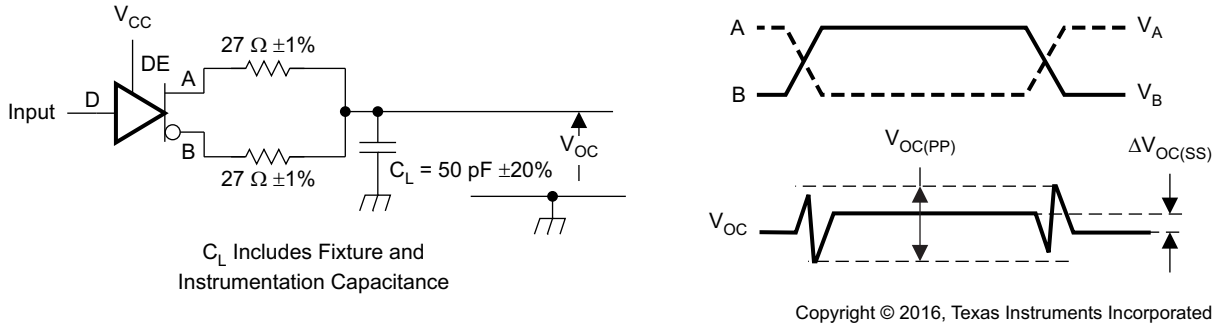
8 Parameter Measurement Information

Input generator rate is 100 kbps, 50% duty cycle, rise or fall time is less than 6 ns, output impedance is 50 Ω.



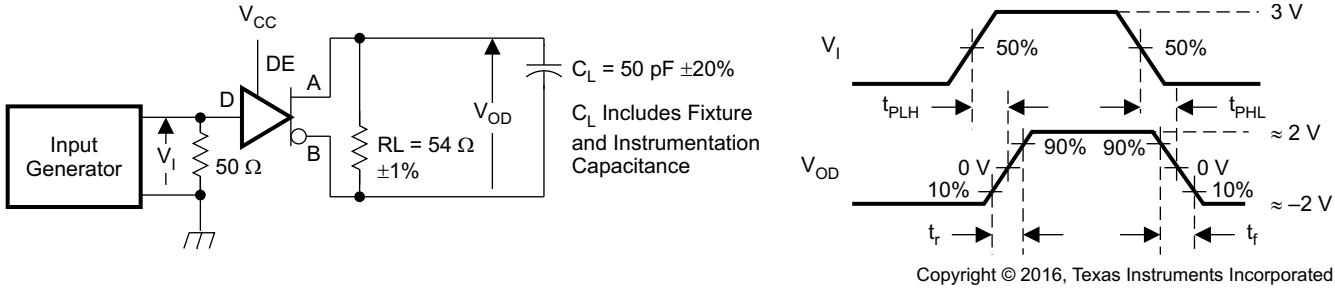
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Figure 6. Measurement of Driver Differential Output Voltage With Common-Mode Load



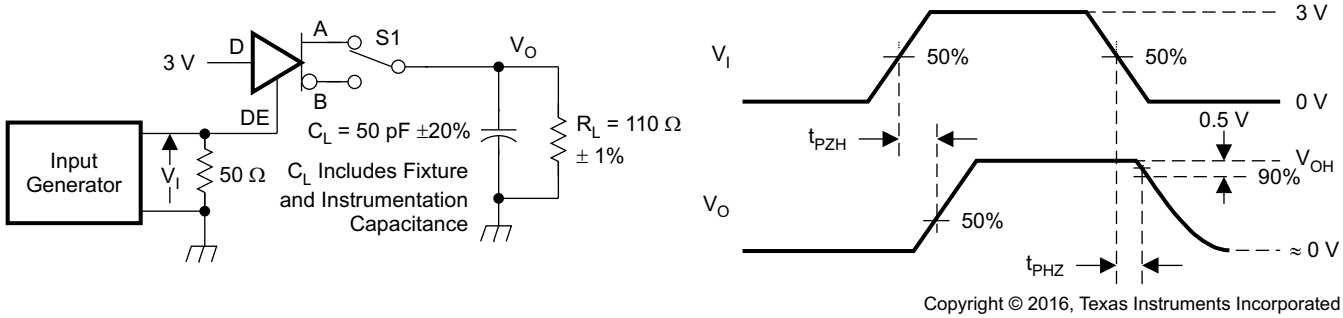
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Figure 7. Measurement of Driver Differential and Common-Mode Output With RS-485 Load



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Figure 8. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays



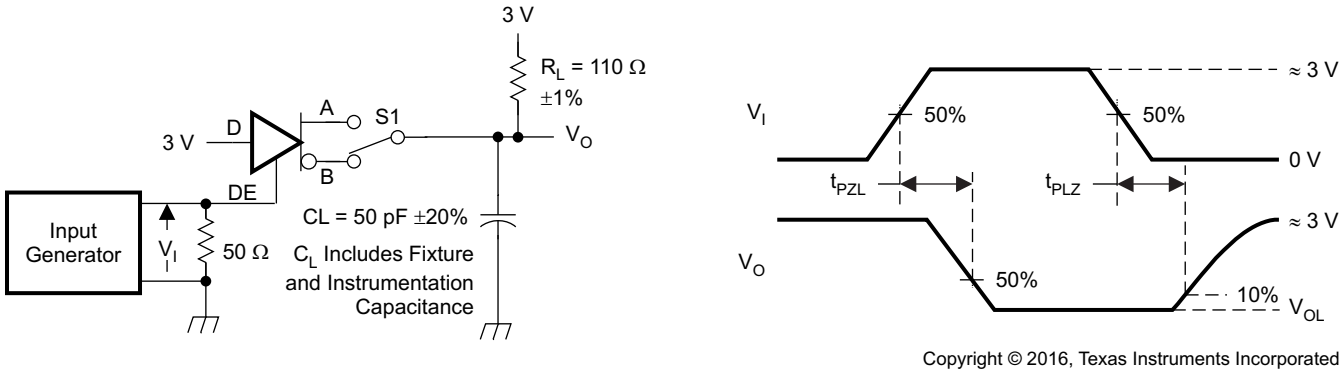
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NOTE: D at 3 V to test non-inverting output, D at 0 V to test inverting output.

Figure 9. Measurement of Driver Enable and Disable Times With Active High Output and Pulldown Load

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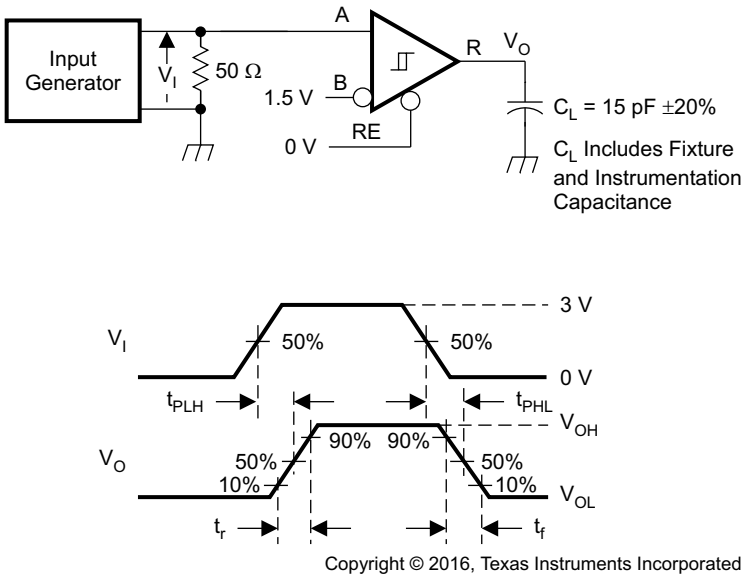
Parameter Measurement Information (continued)



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NOTE: D at 0 V to test non-inverting output, D at 3 V to test inverting output.

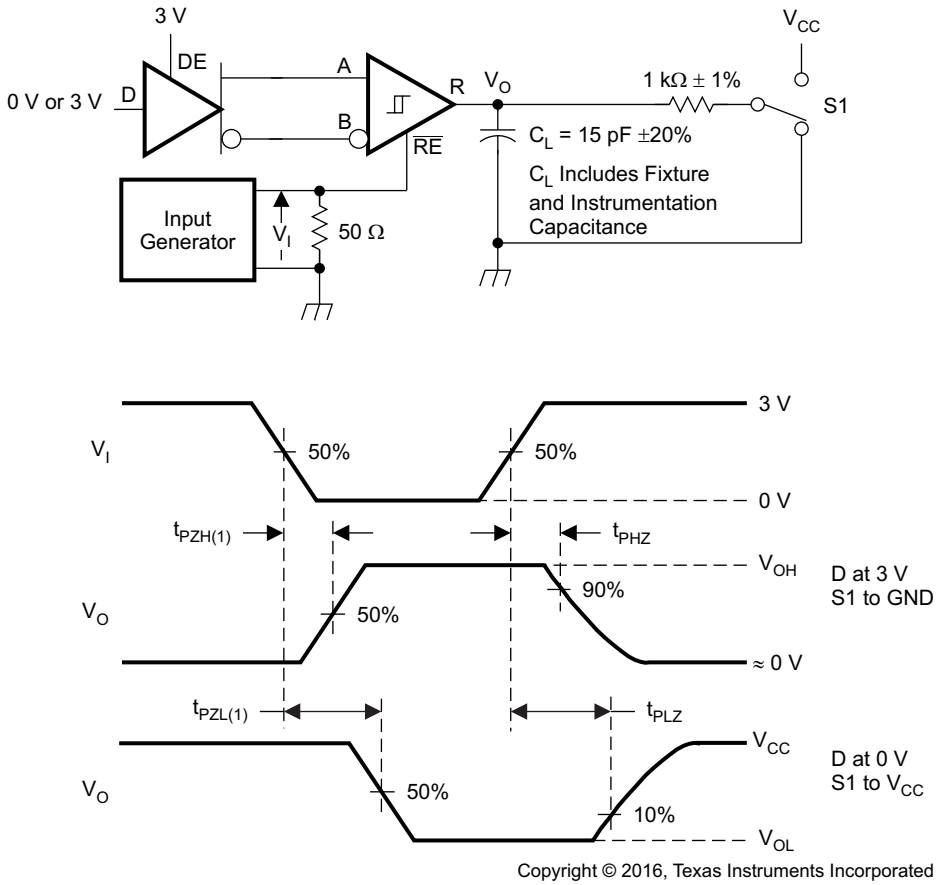
Figure 10. Measurement of Driver Enable and Disable Times With Active-Low Output and Pullup Load



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Figure 11. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

Parameter Measurement Information (continued)

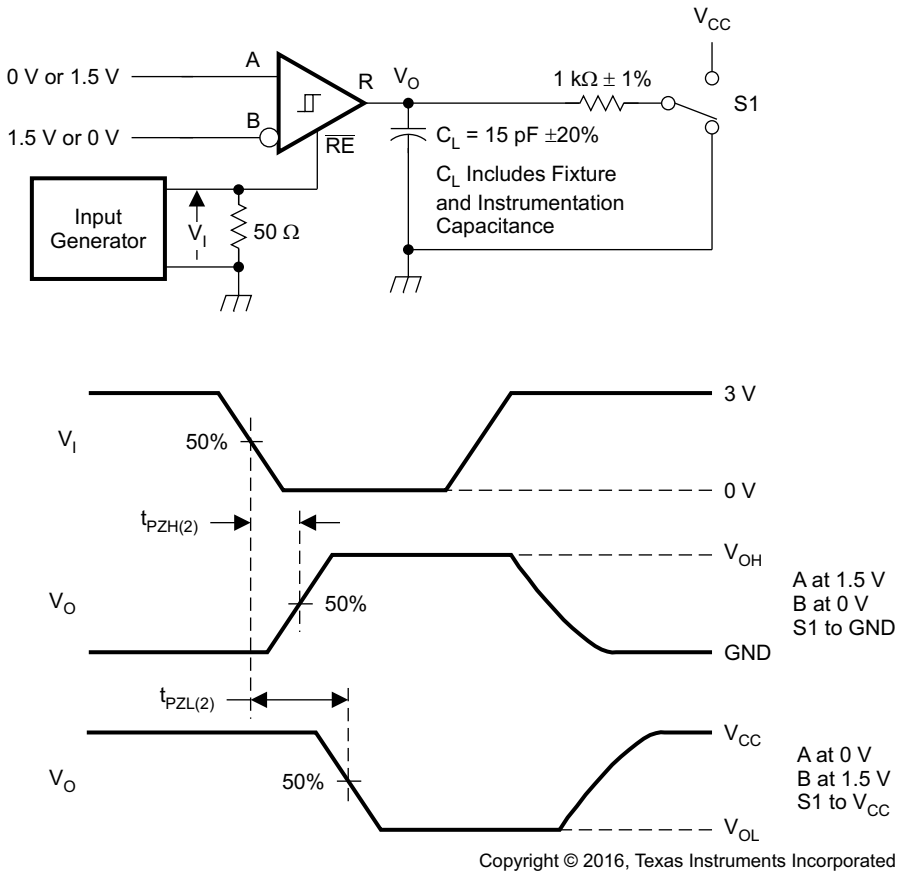


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Figure 12. Measurement of Receiver Enable and Disable Times With Driver Enabled

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Parameter Measurement Information (continued)



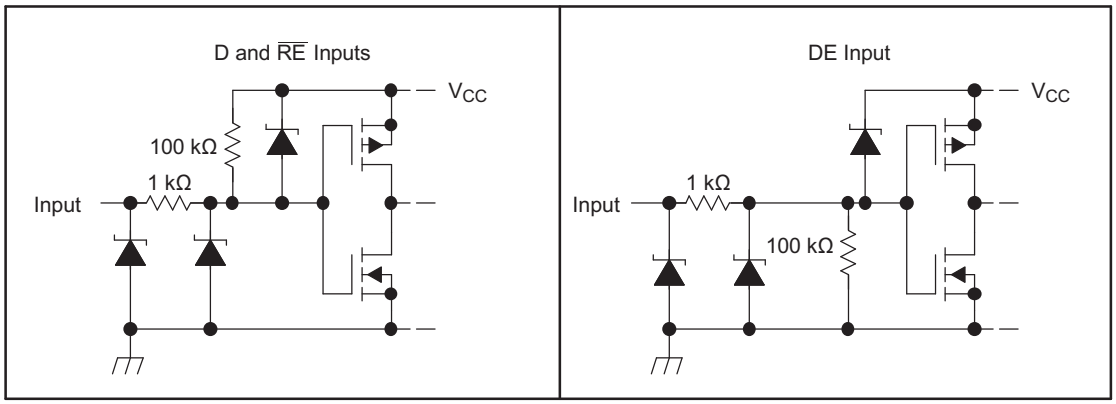
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Figure 13. SN65HVD1781 Measurement of Receiver Enable Times With Driver Disabled

Parameter Measurement Information (continued)

8.1 Equivalent Input Schematic

When the input digital pins float, internal high value resistors pull D/REB pins to V_{CC} and DE pin to GND to place the device into known states. If the voltage level of D/REB input pins is higher than that of power rail, input current can flow through the input resistor and pull up resistor to V_{CC}.



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Figure 14. Equivalent Input Schematic Diagrams

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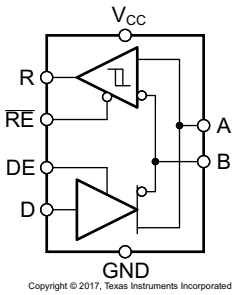
9 Detailed Description

9.1 Overview

The SN65HVD178x devices are half-duplex RS-485 transceivers available in three speed grades suitable for data transmission up to 115 kbps, 1 Mbps, and 10 Mbps.

These devices feature a wide common-mode operating range and bus-pin fault protection up to ±70 V. Each device has an active-HIGH driver enable and active-LOW receiver enable. A standby current of less than 1 µA can be achieved by disabling both driver and receiver.

9.2 Functional Block Diagram



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9.3 Feature Description

Internal ESD protection circuits protect the transceiver bus terminals against ±16 kV human body model (HBM) electrostatic discharges.

Device operation is specified over a wide temperature range from –40°C to 125°C.

9.3.1 70-V Fault Protection

The SN65HVD178x family of RS-485 transceivers is designed to survive bus pin faults up to ±70 V. The SN65HVD1782 will not survive a bus pin fault with a direct short to voltages above 30 V when:

- The device is powered on, AND
- The driver is enabled (DE = HIGH), AND
  - D = HIGH AND the bus fault is applied to the A pin, OR
  - D = LOW AND the bus fault is applied to the B pin

Under other conditions, the device will survive shorts to bus pin faults up to ±70 V. Table 1 summarizes the conditions under which the device may be damaged, and the conditions under which the device will not be damaged.

Table 1. Device Conditions

POWER	DE	D	A	B	RESULTS
OFF	X	X	–70 V < V_A < 70 V	–70 V < V_B < 70 V	Device survives
ON	L	X	–70 V < V_A < 70 V	–70 V < V_B < 70 V	Device survives
ON	H	L	–70 V < V_A < 70 V	–70 V < V_B < 30 V	Device survives
ON	H	L	–70 V < V_A < 70 V	30 V < V_B	Damage may occur
ON	H	H	–70 V < V_A < 30 V	–70 V < V_B < 30 V	Device survives
ON	H	H	30 V < V_A	–70 V < V_B < 30 V	Damage may occur

9.3.2 Receiver Failsafe

The SN65HVD178x family of half-duplex transceivers provides internal biasing of the receiver input thresholds in combination with large input-threshold hysteresis. At a positive input threshold of V_{IT+} = –35 mV and an input hysteresis of V_{HYS} = 30 mV, the receiver output remains logic high under bus-idle, bus-short, or open bus conditions in the presence of up to 130 mV_{PP} differential noise without the need for external failsafe biasing resistors.

9.3.3 Hot-Plugging

These devices are designed to operate in "hot swap" or "hot pluggable" applications. Key features for hot-pluggable applications are power-up and power-down glitch-free operation, default disabled input and output pins, and receiver failsafe.

As shown in Figure 1, an internal power-on reset circuit keeps the driver outputs in a high-impedance state until the supply voltage has reached a level at which the device will reliably operate. This ensures that no problems will occur on the bus pin outputs as the power supply turns on or turns off.

As shown in *Device Functional Modes*, the enable inputs have the feature of default disable on both the driver enable and receiver enable. This ensures that the device will neither drive the bus nor report data on the R pin until the associated controller actively drives the enable pins.

9.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case the differential output voltage defined as $V_{OD} = V_A – V_B$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground, thus, when left open, the driver is disabled (high-impedance) by default. The D pin has an internal pullup resistor to V_{CC}, thus, when left open while the driver is enabled, output A turns high and B turns low.

Table 2. Driver Function Table

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled (1)
X	OPEN	Z	Z	Driver disabled by default (1)
OPEN	H	H	L	Actively drive bus high by default

(1) When both the driver and receiver are disabled, the device enters a low-power standby mode.

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A – V_B$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output, R, turns high. When V_{ID} is negative and lower than the negative input threshold, V_{IT-}, the receiver output, R, turns low. If V_{ID} is between V_{IT+} and V_{IT-} the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

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Table 3. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A - V_B$	$\overline{RE}$	R	
$V_{IT+} < V_{ID}$	L	H	Receive valid bus high
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled (1)
X	OPEN	Z	Receiver disabled by default (1)
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

(1) When both the driver and receiver are disabled, the device enters a low-power standby mode.

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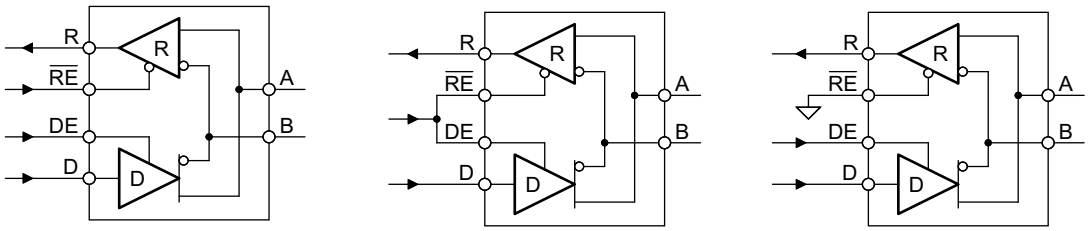
10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN65HVD178x devices are half-duplex RS-485 transceivers commonly used for asynchronous data transmissions. The driver and receiver enable pins allow for the configuration of different operating modes.



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Figure 15. Half-Duplex Transceiver Configurations

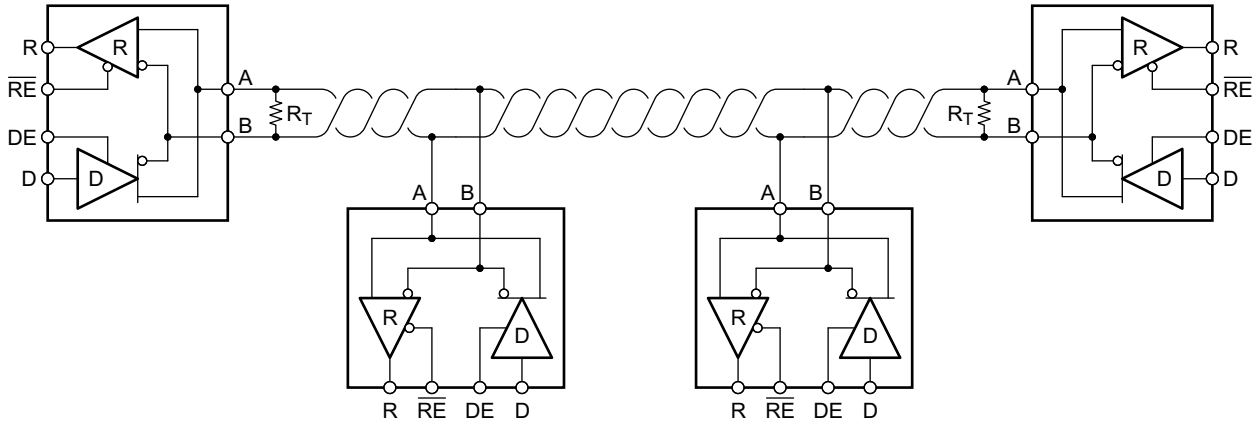
Using independent enable lines provides the most flexible control as it allows for the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows for selective listening into the bus traffic, whether the driver is transmitting data or not.

Combining the enable signals simplifies the interface to the controller by forming a single direction-control signal. In this configuration, the transceiver operates as a driver when the direction-control line is high, and as a receiver when the direction-control line is low.

Additionally, only one line is required when connecting the receiver-enable input to ground and controlling only the driver-enable input. In this configuration, a node not only receives the data from the bus, but also the data it sends and can verify that the correct data have been transmitted.

10.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.



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Figure 16. Typical RS-485 Network With Half-Duplex Transceivers

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Typical Application (continued)

10.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

10.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and bus length, meaning the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable may be without introducing data errors. While most RS-485 systems use data rates from 10 kbps to 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5% or 10%.

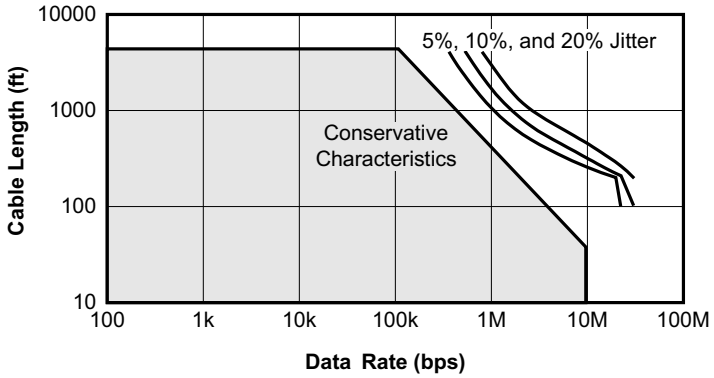


Figure 17. Cable Length vs Data Rate Characteristic

Even higher data rates are achievable (for example, 10 Mbps for the SN65HVD1782) in cases where the interconnect is short enough (or has suitably low attenuation at signal frequencies) to not degrade the data.

10.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in Equation 1.

$$L_{stub} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

10.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. The SN65HVD1780 and SN65HVD1781 are 1/10 unit load transceivers, and so up to 320 can be placed on a common bus. The SN65HVD1782 is a 1/2 unit load transceiver, so up to 64 can share a bus.

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Typical Application (continued)

10.2.1.4 Receiver Failsafe

The differential receivers of the SN65HVD178x family are “failsafe” to invalid bus states caused by:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic High state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the “input indeterminate” range does not include zero volts differential. To comply with the RS-422 and RS-485 standards, the receiver output must output a High when the differential input V_{ID} is more positive than +200 mV, and must output a Low when V_{ID} is more negative than –200 mV. The receiver parameters which determine the failsafe performance are $V_{IT(+)}$, $V_{IT(-)}$, and V_{HYS} (the separation between $V_{IT(+)}$ and $V_{IT(-)}$). As shown in the *Electrical Characteristics*, differential signals more negative than –200 mV will always cause a Low receiver output, and differential signals more positive than +200 mV will always cause a High receiver output.

When the differential input signal is close to zero, it is still above the maximum $V_{IT(+)}$ threshold of –35 mV, and the receiver output will be High. Only when the differential input is more than V_{HYS} below $V_{IT(+)}$ will the receiver output transition to a Low state. Therefore, the noise immunity of the receiver inputs during a bus fault condition includes the receiver hysteresis value, V_{HYS}, as well as the value of $V_{IT(+)}$.

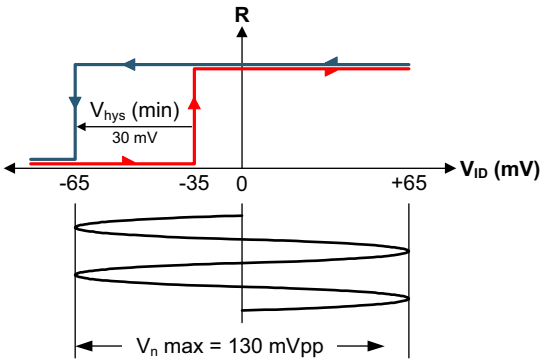


Figure 18. SN65HVD178x Noise Immunity Under Bus Fault Conditions

10.2.2 Detailed Design Procedure

10.2.2.1 Custom Design with WEBENCH® Tools

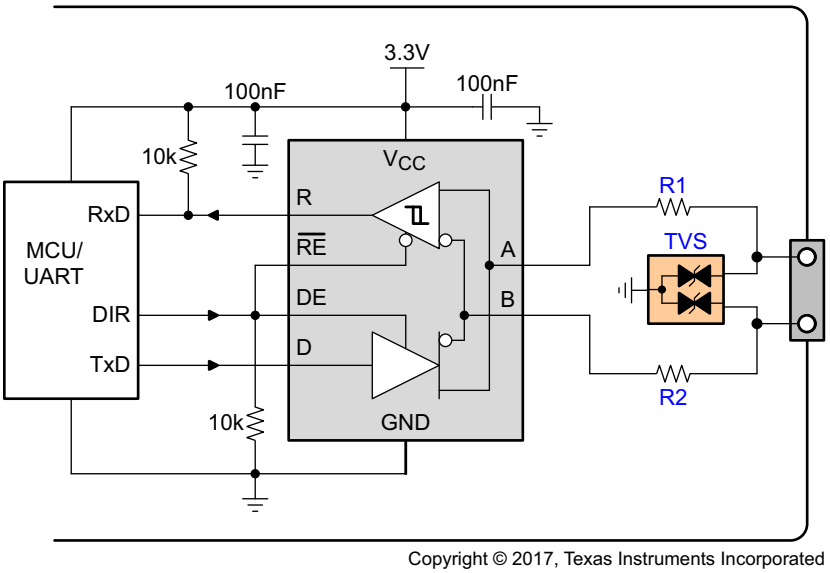
Click here to create a custom design using the SN65HVD178x device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT}, and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. The WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance
   - Run thermal simulations to understand the thermal performance of your board
   - Export your customized schematic and layout into popular CAD formats
   - Print PDF reports for the design, and share your design with colleagues
5. Get more information about WEBENCH tools at www.ti.com/WEBENCH.

Although the SN65HVD178x family is internally protected against human-body-model ESD strikes up to 16 kV, additional protection against higher-energy transients can be provided at the application level by implementing external protection devices.

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Typical Application (continued)



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Figure 19. RS-485 Transceiver With External Transient Protection

Figure 19 shows a protection circuit intended to withstand 8-kV IEC ESD (per IEC 61000-4-2) as well as 4-kV EFT (per IEC 61000-4-4).

Table 4. Bill of Materials

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER
XCVR	RS-485 Transceiver	SN65HVD1781	TI
R1,R2	10 Ω, Pulse-Proof Thick-Film Resistor	CRCW0603010RJNEAHP	Vishay
TVS	Bidirectional 600-W Transient Suppressor	SMBJ43CA	Littelfuse

10.2.3 Application Curve

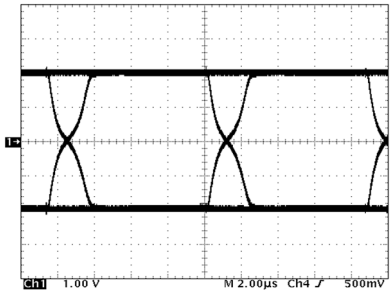


Figure 20. SN65HVD1780 Differential Output at 115 kbps

11 Power Supply Recommendations

To assure reliable operation at all data rates and supply voltages, each supply should be buffered with a 100-nF ceramic capacitor located as close to the supply pins as possible. The TPS76350 is a linear voltage regulator suitable for the 5-V supply.

12 Layout

12.1 Layout Guidelines

On-chip IEC-ESD protection is good for laboratory and portable equipment but often insufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices.

Because ESD and EFT transients have a wide-frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from entering the board.
2. Use VCC and ground planes to provide low-inductance. Note that high-frequency currents follow the path of least inductance and not the path of least impedance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100-nF to 220-nF bypass capacitors as close as possible to the VCC pins of the transceiver, UART, or controller ICs on the board.
5. Use at least two vias for VCC and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
6. Use 1-kΩ to 10-kΩ pullup and pulldown resistors for enable lines to limit noise currents in these lines during transient events.
7. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.

12.2 Layout Example

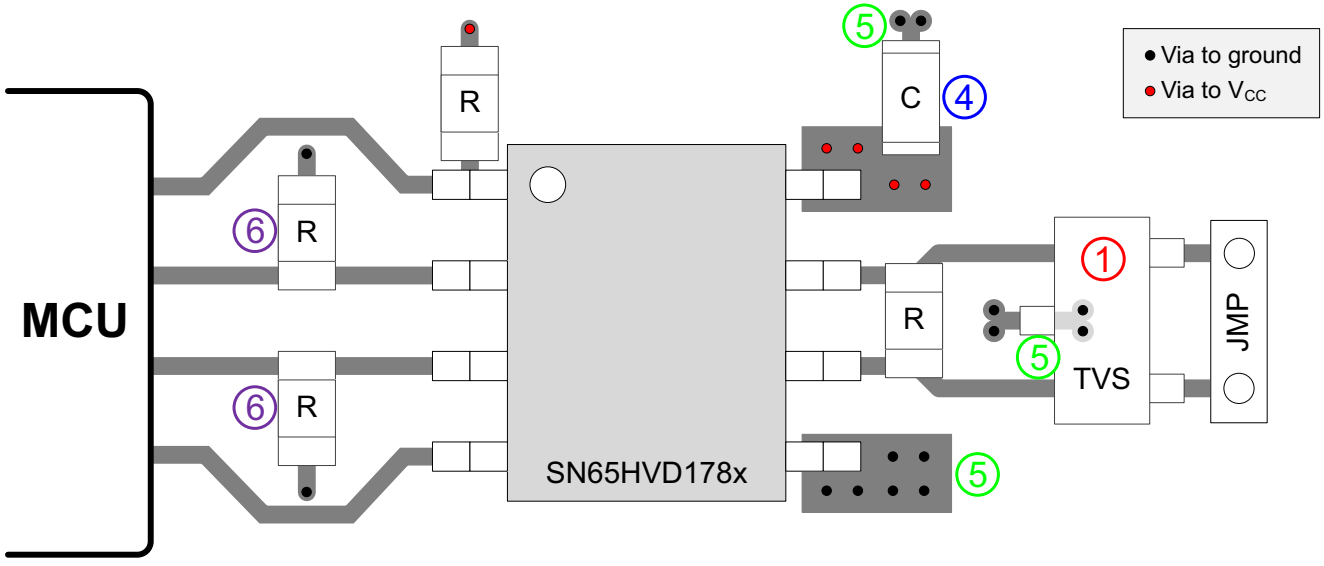


Figure 21. SN65HVD178x Half-Duplex Layout Example

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13 Device and Documentation Support

13.1 Device Support

13.1.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the SN65HVD178x device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT}, and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. The WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance
   - Run thermal simulations to understand the thermal performance of your board
   - Export your customized schematic and layout into popular CAD formats
   - Print PDF reports for the design, and share your design with colleagues
5. Get more information about WEBENCH tools at www.ti.com/WEBENCH.

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13.2 Documentation Support

13.2.1 Related Documentation

For related documentation, see the following:

SN65HVD17xx Fault-Protected RS-485 Transceivers With Extended Common-Mode Range, SLLS872

13.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PART	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN65HVD1780	Click here	Click here	Click here	Click here	Click here
SN65HVD1781	Click here	Click here	Click here	Click here	Click here
SN65HVD1782	Click here	Click here	Click here	Click here	Click here

13.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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13.5 Community Resources

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.6 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
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13.7 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65HVD1780D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1780
SN65HVD1780D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1780
SN65HVD1780D.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1780
SN65HVD1780DG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1780
SN65HVD1780DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1780
SN65HVD1780DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1780
SN65HVD1780DR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1780
SN65HVD1780DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1780
SN65HVD1780P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	65HVD1780
SN65HVD1780P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	65HVD1780
SN65HVD1780P.B	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	65HVD1780
SN65HVD1781D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP1781
SN65HVD1781D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP1781
SN65HVD1781D.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP1781
SN65HVD1781DG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP1781
SN65HVD1781DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP1781
SN65HVD1781DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP1781
SN65HVD1781DR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP1781
SN65HVD1781DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP1781
SN65HVD1781P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	65HVD1781
SN65HVD1781P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	65HVD1781
SN65HVD1781P.B	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	65HVD1781
SN65HVD1782D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1782
SN65HVD1782D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1782
SN65HVD1782DG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1782
SN65HVD1782DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1782
SN65HVD1782DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1782
SN65HVD1782DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1782
SN65HVD1782P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	65HVD1782

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65HVD1782P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	65HVD1782

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN65HVD1780, SN65HVD1781, SN65HVD1782 :

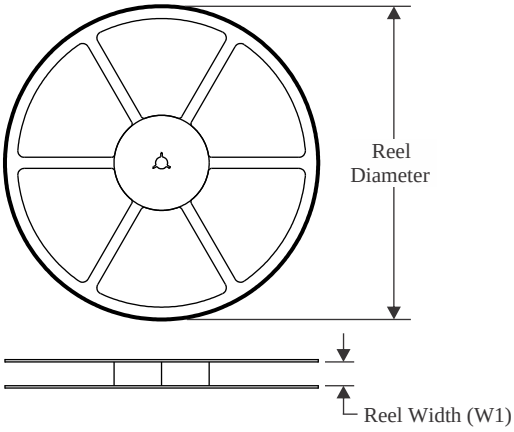
- Automotive : SN65HVD1780-Q1, SN65HVD1781-Q1, SN65HVD1782-Q1

NOTE: Qualified Version Definitions:

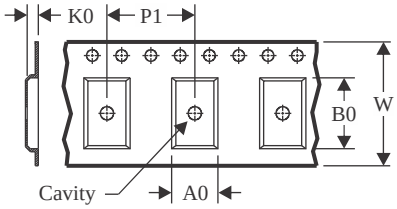
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

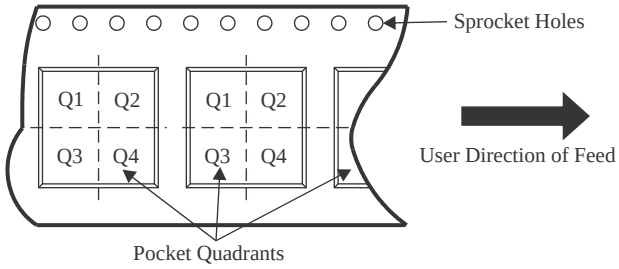


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

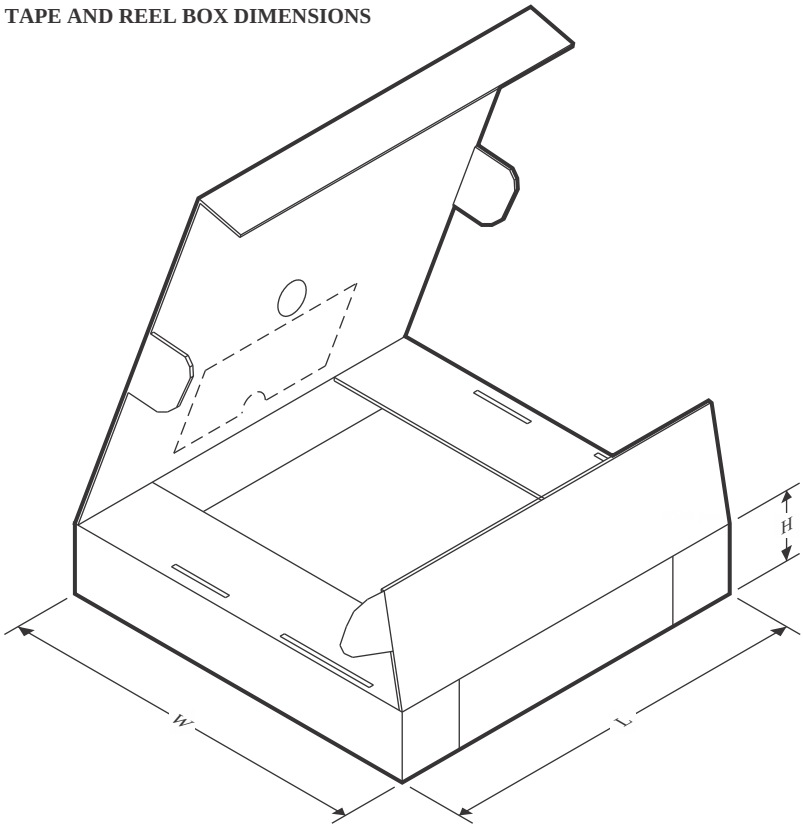
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD1780DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD1781DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD1782DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

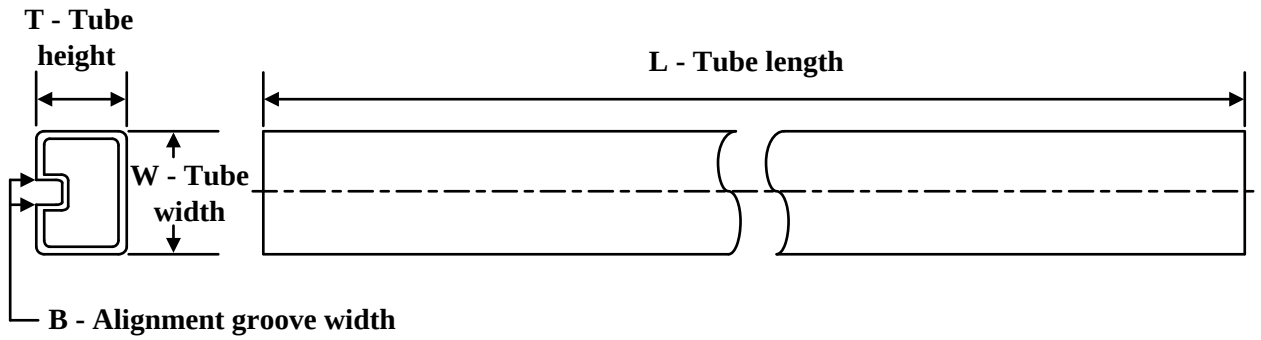
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

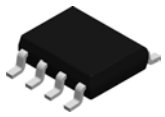
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD1780DR	SOIC	D	8	2500	353.0	353.0	32.0
SN65HVD1781DR	SOIC	D	8	2500	353.0	353.0	32.0
SN65HVD1782DR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65HVD1780D	D	SOIC	8	75	506.6	8	3940	4.32
SN65HVD1780D.A	D	SOIC	8	75	506.6	8	3940	4.32
SN65HVD1780D.B	D	SOIC	8	75	506.6	8	3940	4.32
SN65HVD1780DG4	D	SOIC	8	75	506.6	8	3940	4.32
SN65HVD1780P	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD1780P.A	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD1780P.B	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD1781D	D	SOIC	8	75	506.6	8	3940	4.32
SN65HVD1781D.A	D	SOIC	8	75	506.6	8	3940	4.32
SN65HVD1781D.B	D	SOIC	8	75	506.6	8	3940	4.32
SN65HVD1781DG4	D	SOIC	8	75	506.6	8	3940	4.32
SN65HVD1781P	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD1781P.A	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD1781P.B	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD1782D	D	SOIC	8	75	506.6	8	3940	4.32
SN65HVD1782D.A	D	SOIC	8	75	506.6	8	3940	4.32
SN65HVD1782DG4	D	SOIC	8	75	506.6	8	3940	4.32
SN65HVD1782P	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD1782P.A	P	PDIP	8	50	506	13.97	11230	4.32

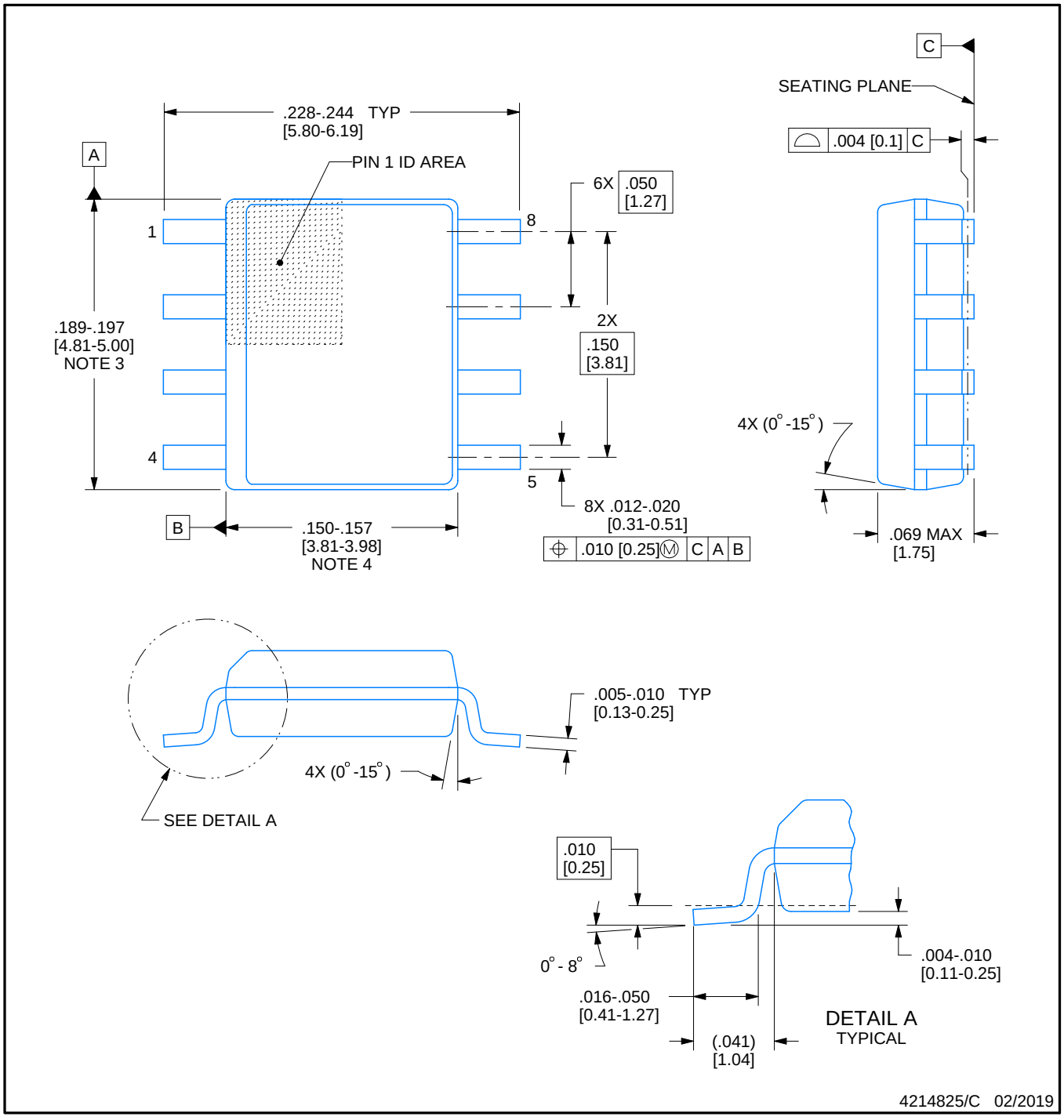


PACKAGE OUTLINE

D0008A

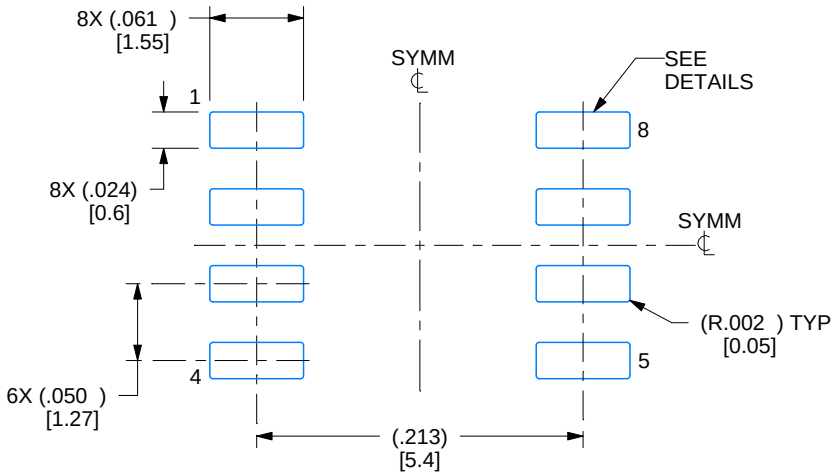
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

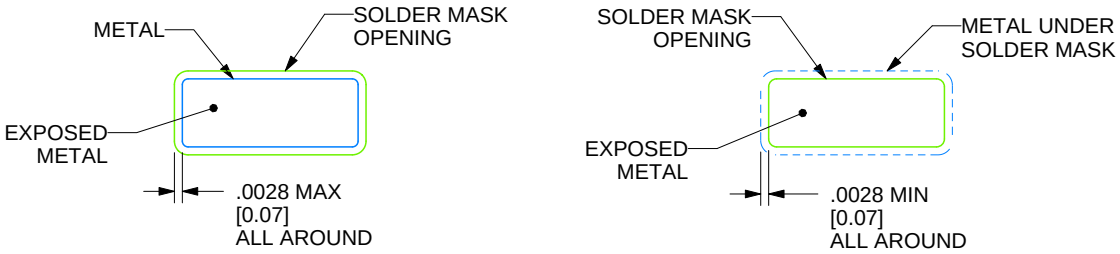


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

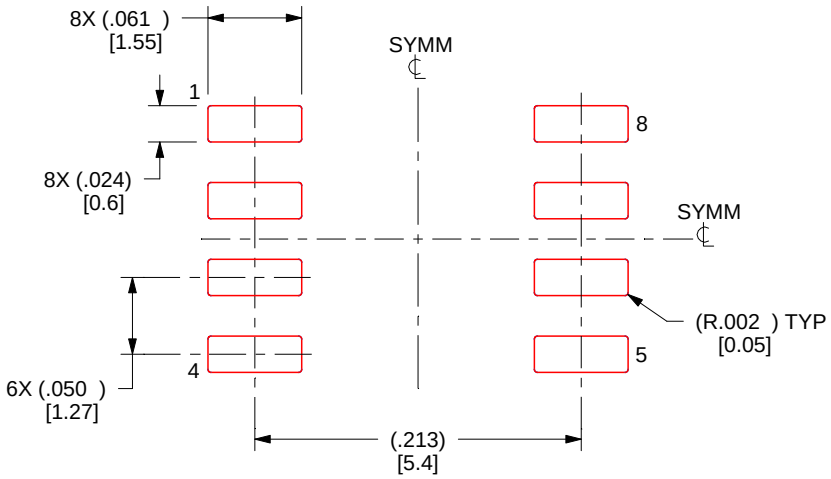
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



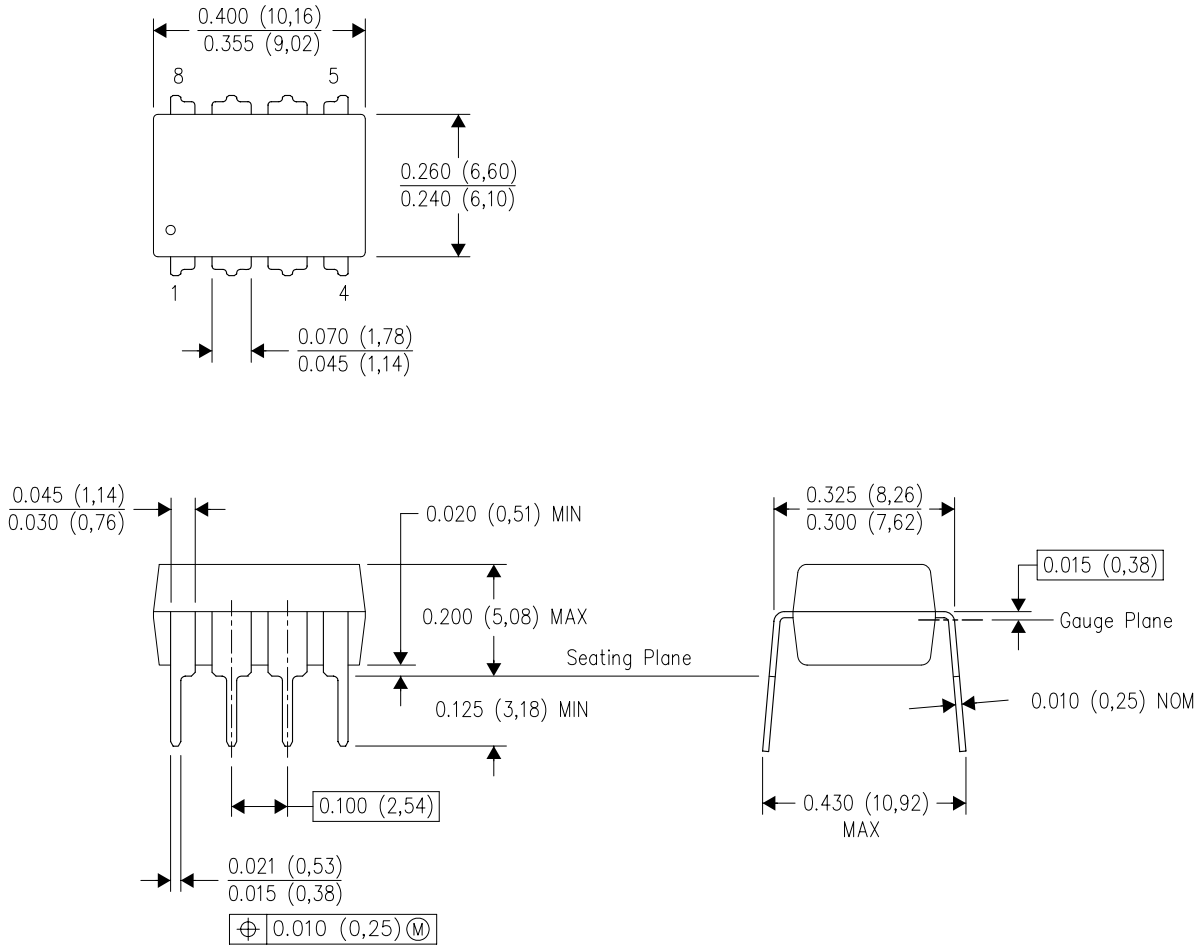
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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