SN65HVD1785, SN65HVD1786, SN65HVD1787
SN65HVD1791, SN65HVD1792, SN65HVD1793
SLLS872J – JANUARY 2008 – REVISED MARCH 2023

SN65HVD17xx Fault-Protected RS-485 Transceivers With Extended Common-Mode Range

1 Features

- Bus-Pin Fault Protection to:
  - > ±70 V ('HVD1785, 86, 91, 92)
  - > ±30 V ('HVD1787, 93)
- Common-Mode Voltage Range (–20 V to 25 V) More Than Doubles TIA/EIA 485 Requirement
- Bus I/O Protection
  - ±16 kV JEDEC HBM Protection
- Reduced Unit Load for Up to 256 Nodes
- Failsafe Receiver for Open-Circuit, Short-Circuit and Idle-Bus Conditions
- Low Power Consumption
  - Low Standby Supply Current, 1 µA Typical
  - I_{CC} 5 mA Quiescent During Operation
- Power-Up, Power-Down Glitch-Free Operation

2 Applications

- Designed for RS-485 and RS-422 Networks

3 Description

These devices are designed to survive overvoltage faults such as direct shorts to power supplies, mis-wiring faults, connector failures, cable crushes, and tool mis-applications. They are also robust to ESD events, with high levels of protection to human-body model specifications.

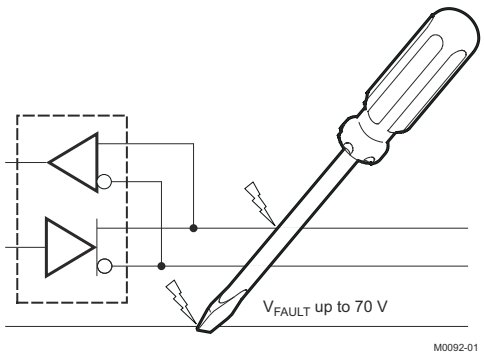
These devices combine a differential driver and a differential receiver, which operate from a single power supply. In the 'HVD1785, 'HVD1786, and 'HVD1787, the driver differential outputs and the receiver differential inputs are connected internally to form a bus port suitable for half-duplex (two-wire bus) communication. In the 'HVD1793, the driver differential outputs and the receiver differential inputs are separate pins, to form a bus port suitable for full-duplex (four-wire bus) communication. These ports feature a wide common-mode voltage range, making the devices suitable for multipoint applications over long cable runs. These devices are characterized from –40°C to 105°C.

For similar features with 3.3-V supply operation, see the SN65HVD1781 (SLLS877).

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
SN65HVD1785, SN65HVD1786, SN65HVD1787	SOIC (8)	4.90 mm × 3.91 mm
	PDIP (8)	9.81 mm × 6.35 mm
SN65HVD1791, SN65HVD1792, SN65HVD1793	SOIC (14)	8.65 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



Example of Bus Short to Power Supply

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (August 2015) to Revision J (March 2023) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document....1

Changes from Revision H (February 2010) to Revision I (August 2015) **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

Changes from Revision G (April 2009) to Revision H (February 2010) **Page**

- Deleted 70-V from the data sheet title.... 1
- Changed first Features Bullet From: Bus-Pin Fault Protection to > ±70 V To: Bus-Pin Fault Protection to: > ±70 V ('HVD1785, 86,91,92), > ±30 V ('HVD1787, 93)....1
- Changed Voltage range at A and B inputs in the ABS MAX RATINGS table, adding seperate conditions for the different devices....6
- Changed From: Voltage input range, transient pulse, A and B, through 100 Ω To: Transient overvoltage pulse through 100 Ω per TIA-485....6
- Added the 70-V Fault-Protection section.... 16

Changes from Revision F (November 2008) to Revision G (April 2009) **Page**

- Added I_{OH} = –400 µA conditions and values to the Receiver high-level output voltage.... 7
- Added Receiver enabled V_{CM} > V_{CC} 9
- Added Receiver Failsafe information....15
- Changed the *Receiver Failsafe* section.... 16

Changes from Revision E (July 2008) to Revision F (November 2008) **Page**

- Added to Title: With Extended Common-Mode Range.... 1

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- Added Receiver enabled V_{CM} > V_{CC} condition and values to the Driver enabled time 9
- Added Figure 7-4 10

Changes from Revision D (June 2008) to Revision E (July 2008) **Page**

- Changed - Removed Product Preview label.....4
- Changed SN65HVD1792 Removed Product Preview label..... 4
- Changed SN65HVD1793 Removed Product Preview label..... 4

Changes from Revision C (March 2008) to Revision D (June 2008) **Page**

- Added Features Bullet: Power-Up, Power-Down Glitch-Free Operation..... 1
- Changed (Preview) to part number SN65HVD1791 in the Product Selection Guide..... 4
- Added section - APPLICATION INFORMATION..... 15
- Changed Receiver disabled by default - Enable from X to OPEN. Output from OPEN to Z..... 18

Changes from Revision B (March 2008) to Revision C (March 2008) **Page**

- Changed Rec Op Table. Signaling rate, HVD1787, HVD1793 From: 20 Mbps max to 10 Mbps max.....6

Changes from Revision A (March 2008) to Revision B (March 2008) **Page**

- Added T_A ≤ 85°C and T_A ≤ 105°C conditions and values to the Receiver low-level output voltage.....7
- Changed the max value for Supply Current (quiescent) Driver and receiver disabled, From 1 µA To 5 µA.....7

Changes from Revision * (January 2008) to Revision A (March 2008) **Page**

- Changed Features Bullet From: Low Standby Supply Current, 2 µA Max To: Low Standby Supply Current, 1 µA Typ.....1
- Deleted columns to the PRODUCT SELECTION GUIDE for Package Options and Status.....4
- Added text: For similar features with 3.3 V supply operation.....4
- Changed the Product Selection Guide Signaling Rate for SN65HVD1787 From 20 Mbps To: 10 Mbps..... 4
- Changed the Product Selection Guide Signaling Rate for SN65HVD1793 From 20 Mbps To: 10 Mbps..... 4
- Deleted The Competitive Comparison table.....6
- Added $|V_{OD}|$ RS-485 with common-mode load T_A ≤ 85°C and T_A ≤ 105°C.....7
- Changed ΔV_{OC} From min = -0.2 mV and max 0.2 mV To: min = -100 mV and max 100 mV.....7
- Changed HVD1785/1791 Driver differential output rise/fall time max value From 2.5 µs To: 2.6 µs.....9
- Changed HVD1787/1793 Driver differential output rise/fall time max value From 1.5 ns To: 30 ns.....9
- Changed Receiver propagation delay max value From 50 ns To: 70 ns.....9
- Changed t_{PLZ}, t_{PHZ} Receiver disable time From 3000 ns To 100 ns.....9
- Deleted graph DIFFERENTIAL OUTPUT VOLTAGE vs DIFFERENTIAL LOAD CURRENT..... 10

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5 Product Selection Guide

PART NUMBER	DUPLEX	SIGNALING RATE	NODES	CABLE LENGTH
SN65HVD1785	Half	115 kbps	Up to 256	1500 m
SN65HVD1786	Half	1 Mbps	Up to 256	150 m
SN65HVD1787	Half	10 Mbps	Up to 64	50 m
SN65HVD1791	Full	115 kbps	Up to 256	1500 m
SN65HVD1792	Full	1 Mbps	Up to 256	150 m
SN65HVD1793	Full	10 Mbps	Up to 64	50 m

6 Pin Configuration and Functions

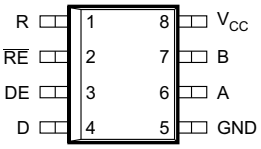
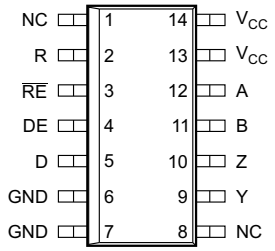


Figure 6-1. D or P Package
8-Pin SOIC or PDIP
SN65HVD1785, 1786, 1787 (Top View)

Pin Functions (SN65HVD1785, SN65HVD1786, SN65HVD1787)

PIN		TYPE	DESCRIPTION
NAME	NO.		
A	6	Bus input/ output	Driver output or receiver input (complementary to B)
B	7	Bus input/ output	Driver output or receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable, active high
GND	5	Reference potential	Local device ground
R	1	Digital output	Receive data output
$\overline{RE}$	2	Digital input	Receiver enable, active low
V_{CC}	8	Supply	4.5-V-to-5.5-V supply

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NC - No internal connection

Pins 6 and 7 are connected together internally.

Pins 13 and 14 are connected together internally.

Figure 6-2. D Package
14-Pin SOIC
SN65VD1791, 1792, 1793 (Top View)

Pin Functions (SN65HVD1791, SN65HVD1792, SN65HVD1793)

PIN		TYPE	DESCRIPTION
NAME	NO.		
A	12	Bus input	Receiver input (complementary to B)
B	11	Bus input	Receiver input (complementary to A)
Y	9	Bus output	Driver output (complementary to Z)
Z	10	Bus output	Driver output (complementary to Y)
D	5	Digital input	Driver data input
DE	4	Digital input	Driver enable, active high
GND	6, 7	Reference potential	Local device ground
R	2	Digital output	Receive data output
$\overline{RE}$	3	Digital input	Receiver enable, active low
V_{CC}	13, 14	Supply	4.5-V to 5.5-V supply
NC	1, 8	No connect	No connect; should be left floating

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7 Specifications

7.1 Absolute Maximum Ratings[1]

				MIN	MAX	UNIT
V_{CC}	Supply voltage			–0.5	7	V
	Voltage at bus pins	'HVD1785, 86, 91, 92, 93	A, B pins	–70	70	V
		'HVD1787	A, B pins	–70	30	V
		'HVD1793	Y, Z pins	–70	30	V
	Input voltage at any logic pin			–0.3	V_{CC} + 0.3	V
	Transient overvoltage pulse through 100 Ω per TIA-485			–100	100	V
	Receiver output current			–24	24	mA
T_J	Junction temperature				170	°C
T_{stg}	Storage temperature				160	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1], JEDEC Standard 22, Test Method A114	Bus terminals and GND	±16000	V
			All pins	±4000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2], JEDEC Standard 22, Test Method C101		±2000	
		Machine Model, JEDEC Standard 22, Test Method A115		±400	
		IEC 60749-26 ESD (human-body model)	Bus terminals and GND	±16000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_I	Input voltage at any bus terminal (separately or common mode)[1]		–20		25	V
V_{IH}	High-level input voltage (driver, driver enable, and receiver enable inputs)		2		V_{CC}	V
V_{IL}	Low-level input voltage (driver, driver enable, and receiver enable inputs)		0		0.8	V
V_{ID}	Differential input voltage		–25		25	V
I_O	Output current, driver		–60		60	mA
	Output current, receiver		–8		8	mA
R_L	Differential load resistance		54	60		Ω
C_L	Differential load capacitance			50		pF
$1/t_{UI}$	Signaling rate	HVD1785, HVD1791			115	kbps
		HVD1786, HVD1792			1	Mbps
		HVD1787, HVD1793			10	Mbps
T_A	Operating free-air temperature (see application section for thermal information)		–40		105	°C
T_J	Junction temperature		–40		150	°C

(1) By convention, the least positive (most negative) limit is designated as minimum in this data sheet.

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7.4 Thermal Information

THERMAL METRIC[1]		SN65HVD1785, SN65HVD1786, SN65HVD1787		SN65HVD1791, SN65HVD1792, SN65HVD1793	UNIT
		D (SOIC)	P (PDIP)	D (SOIC)	
		8 PINS	8 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	138	59	95	°C/W
$R_{\theta JA\ (low\text{-}K)}$	Junction-to-case (top) thermal resistance	242	128	168	°C/W
$R_{\theta JC(top)}$	Junction-to-board thermal resistance	61	61	44	°C/W
$R_{\theta JB}$	Junction-to-top characterization parameter	62	39	40	°C/W
ψ_{JT}	Junction-to-board characterization parameter	3.4	17.6	8.2	°C/W
ψ_{JB}	Junction-to-case (bottom) thermal resistance	33.4	28.3	25	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$\lvert V_{OD}\rvert$	Driver differential output voltage magnitude	RS-485 with common-mode load, V_{CC} > 4.75 V, see Figure 8-1	$T_A \le 85°C$		1.5			V
			$T_A \le 105°C$		1.4			
		R_L = 54 Ω, 4.75 V ≤ V_{CC} ≤ 5.25 V			1.5	2		
		R_L = 100 Ω, 4.75 V ≤ V_{CC} ≤ 5.25 V			2	2.5		
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of driver differential output voltage	R_L = 54 Ω			–0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage				1	V_{CC}/2	3	V
ΔV_{OC}	Change in differential driver output common-mode voltage				–100	0	100	mV
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage	Center of two 27-Ω load resistors, see Figure 8-2				500		mV
C_{OD}	Differential output capacitance					23		pF
V_{IT+}	Positive-going receiver differential input voltage threshold	V_{CM} = –20 V to 25 V				–100	–10	mV
$V_{IT–}$	Negative-going receiver differential input voltage threshold				–200	–150		mV
V_{HYS}	Receiver differential input voltage threshold hysteresis ($V_{IT+} – V_{IT–}$)				30	50		mV
V_{OH}	Receiver high-level output voltage	I_{OH} = –8 mA			2.4	V_{CC} – 0.3		V
		I_{OH} = –400 µA			4			
V_{OL}	Receiver low-level output voltage	I_{OL} = 8 mA	$T_A \le 85°C$			0.2	0.4	V
			$T_A \le 105°C$			0.2	0.5	
I_I	Driver input, driver enable, and receiver enable input current				–100		100	µA
I_{OZ}	Receiver output high-impedance current	V_O = 0 V or V_{CC}, $\overline{RE}$ at V_{CC}			–1		1	µA
I_{OS}	Driver short-circuit output current				–250		250	mA
I_I	Bus input current (disabled driver)	V_{CC} = 4.5 to 5.5 V or V_{CC} = 0 V, DE at 0 V	85, 86, 91, 92	V_I = 12 V		75	125	µA
				V_I = –7 V	–100	–40		
			87, 93	V_I = 12 V			500	
				V_I = –7 V	–400			

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7.5 Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC}	Supply current (quiescent)	Driver and receiver enabled	DE = V_{CC}, RE = GND, no load		4	6	mA
		Driver enabled, receiver disabled	DE = V_{CC}, RE = V_{CC}, no load		3	5	
		Driver disabled, receiver enabled	DE = GND, RE = GND, no load		2	4	
		Driver and receiver disabled	DE = GND, D = open RE = V_{CC}, no load		0.5	5	µA
	Supply current (dynamic)	See *Section 7.8*					

7.6 Thermal Considerations

PARAMETER			TEST CONDITIONS	VALUE	UNIT
P_D	Power dissipation	85, 91	V_{CC} = 5.5 V, T_J = 150°C, R_L = 300 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 5-V supply, unterminated(1)	290	mW
		85, 91	V_{CC} = 5.5 V, T_J = 150°C, R_L = 100 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 5-V supply, RS-422 load(1)	320	
		86			
		87			
		85, 91	V_{CC} = 5.5 V, T_J = 150°C, R_L = 54 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver) 5-V supply, RS-485 load(1)	400	
		86			
		87			
T_{SD}	Thermal-shutdown junction temperature			170	°C

(1) Driver and receiver enabled, 50% duty cycle square-wave signal at signaling rate: HVD1785, 1791 at 115 kbps, HVD1786 at 1 Mbps, HVD1787 at 10 Mbps)

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7.7 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER (HVD1785 AND HVD1791)							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF, see Figure 8-3		0.4	1.7	2.6	µs
t_{PHL}, t_{PLH}	Driver propagation delay				0.8	2	µs
$t_{SK(P)}$	Driver differential output pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$				20	250	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 8-4 and Figure 8-5		0.1	5	µs
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			0.2	3	µs
		Receiver disabled			3	12	
DRIVER (HVD1786 AND HVD1792)							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF, see Figure 8-3		50		300	ns
t_{PHL}, t_{PLH}	Driver propagation delay					200	ns
$t_{SK(P)}$	Driver differential output pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$					25	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 8-4 and Figure 8-5			3	µs
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled				300	ns
		Receiver disabled				10	µs
		Receiver enabled	$V_{CM} > V_{CC}$		500		ns
DRIVER (HVD1787 AND HVD1793)							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF, see Figure 8-3		3		30	ns
t_{PHL}, t_{PLH}	Driver propagation delay					50	ns
$t_{SK(P)}$	Driver differential output pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$					10	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 8-4 and Figure 8-5			3	µs
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled				300	ns
		Receiver disabled				9	µs
		Receiver enabled	$V_{CM} > V_{CC}$		500		ns
RECEIVER (ALL DEVICES UNLESS OTHERWISE NOTED)							
t_r, t_f	Receiver output rise/fall time	C_L = 15 pF, see Figure 8-6			4	15	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time		85, 86, 91, 92		100	200	ns
			87, 93			70	
$t_{SK(P)}$	Receiver output pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$		85, 86, 91, 92		6	20	ns
			87, 93			5	
t_{PLZ}, t_{PHZ}	Receiver disable time	Driver enabled, see Figure 8-7			15	100	ns
$t_{PZL(1)}$, $t_{PZH(1)}$ $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time	Driver enabled, see Figure 8-7			80	300	ns
		Driver disabled, see Figure 8-8			3	9	µs

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7.8 Typical Characteristics

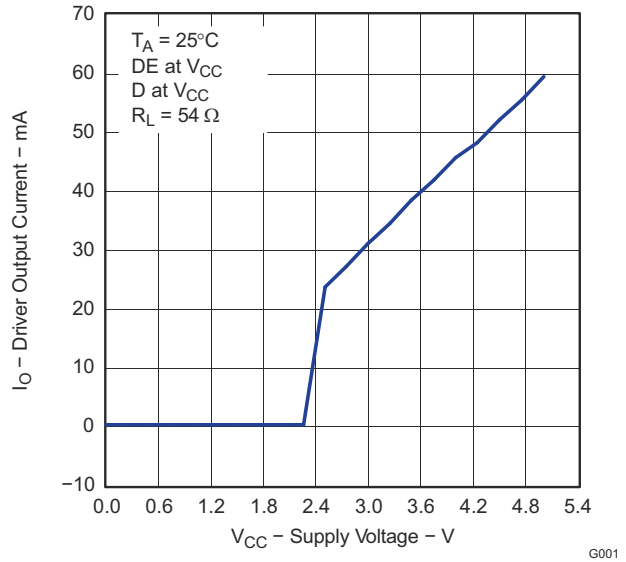


Figure 7-1. Driver Output Current vs Supply Voltage

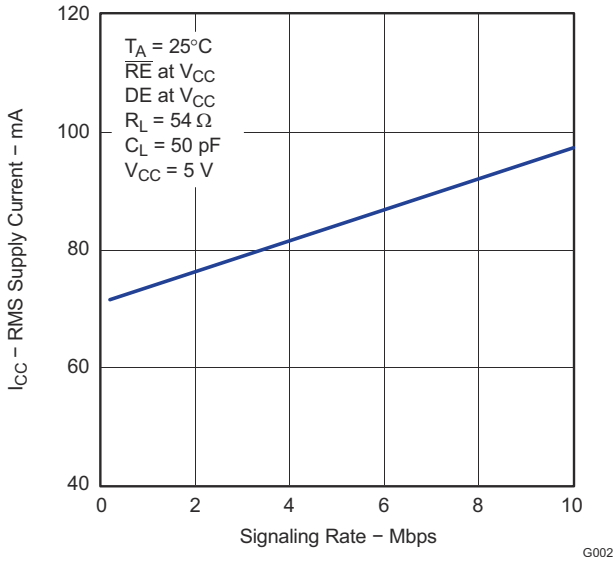


Figure 7-2. HVD1787 RMS Supply Current vs Signaling Rate

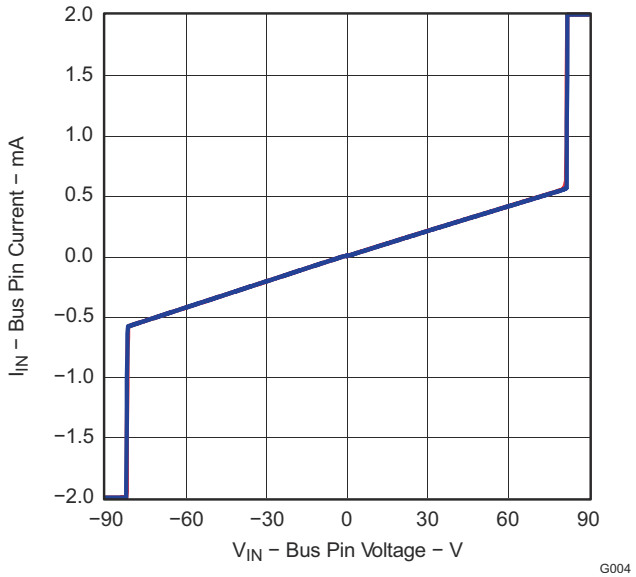


Figure 7-3. Bus Pin Current vs Bus Pin Voltage

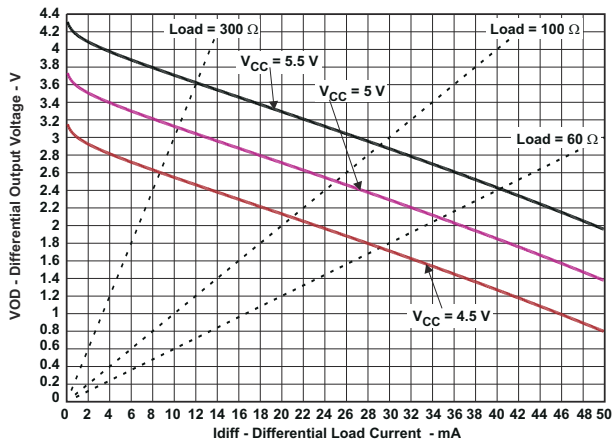


Figure 7-4. Differential Output Voltage vs. Differential Load Current

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8 Parameter Measurement Information

Input generator rate is 100 kbps, 50% duty cycle, rise and fall times less than 6 nsec, output impedance 50 Ω.

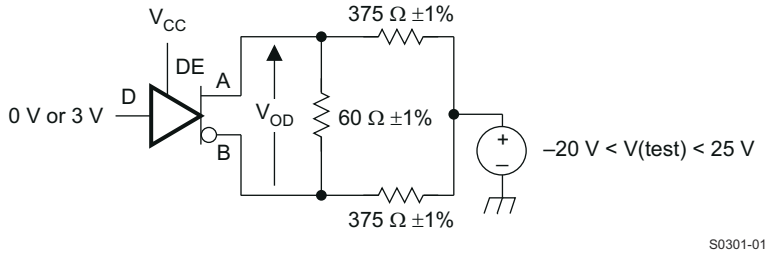


Figure 8-1. Measurement of Driver Differential Output Voltage With Common-Mode Load

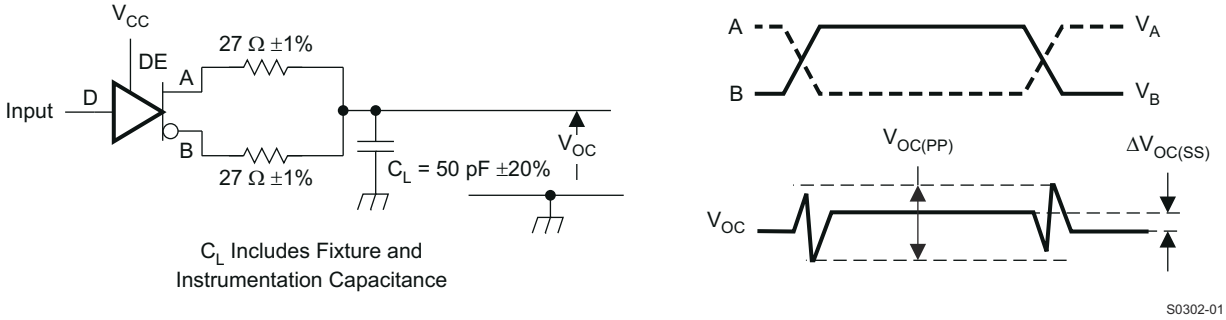


Figure 8-2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

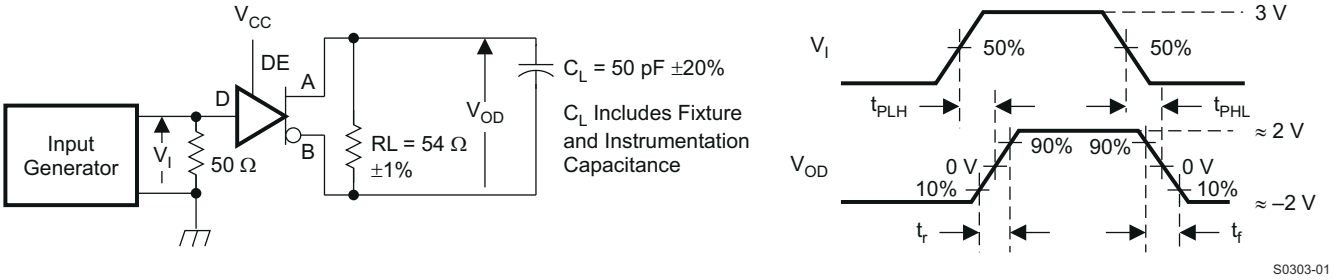
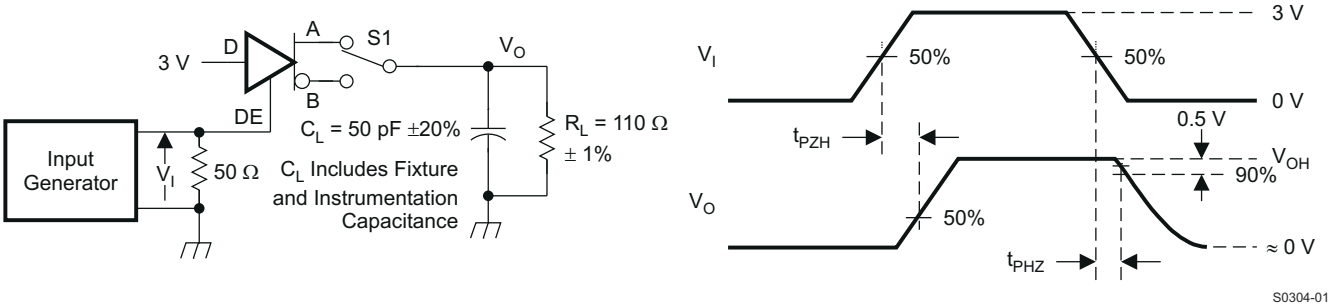
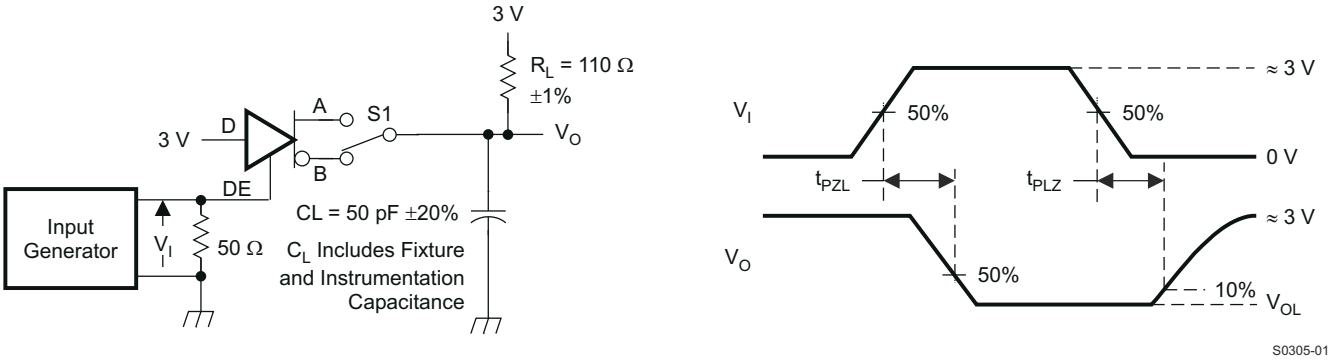


Figure 8-3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays



D at 3 V to test non-inverting output, D at 0 V to test inverting output.

Figure 8-4. Measurement of Driver Enable and Disable Times With Active High Output and Pulldown Load



D at 0 V to test non-inverting output, D at 3 V to test inverting output.

Figure 8-5. Measurement of Driver Enable and Disable Times With Active-Low Output and Pullup Load

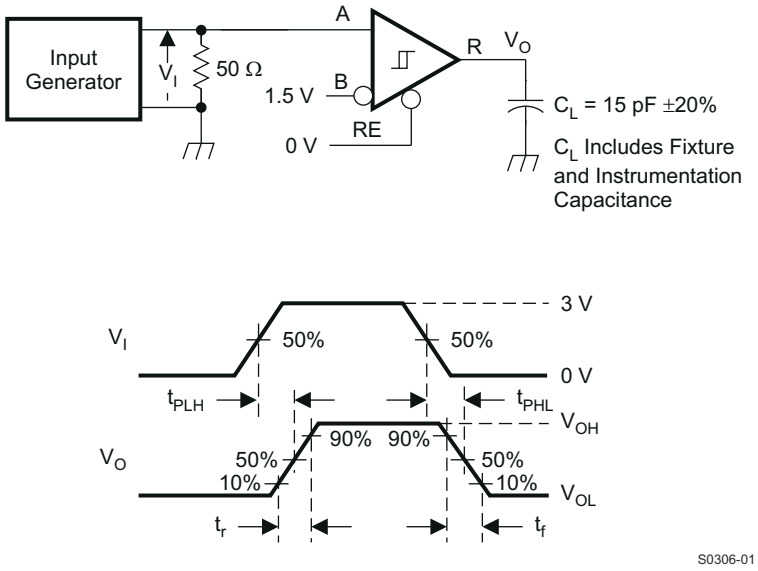


Figure 8-6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

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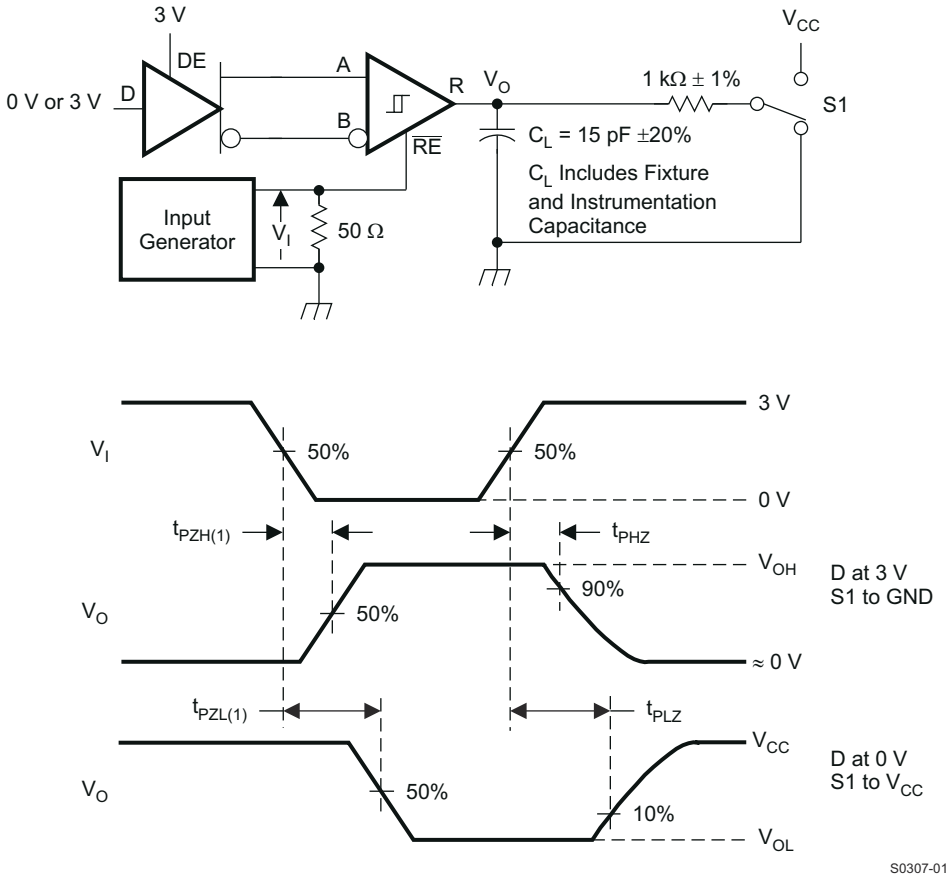


Figure 8-7. Measurement of Receiver Enable/Disable Times With Driver Enabled

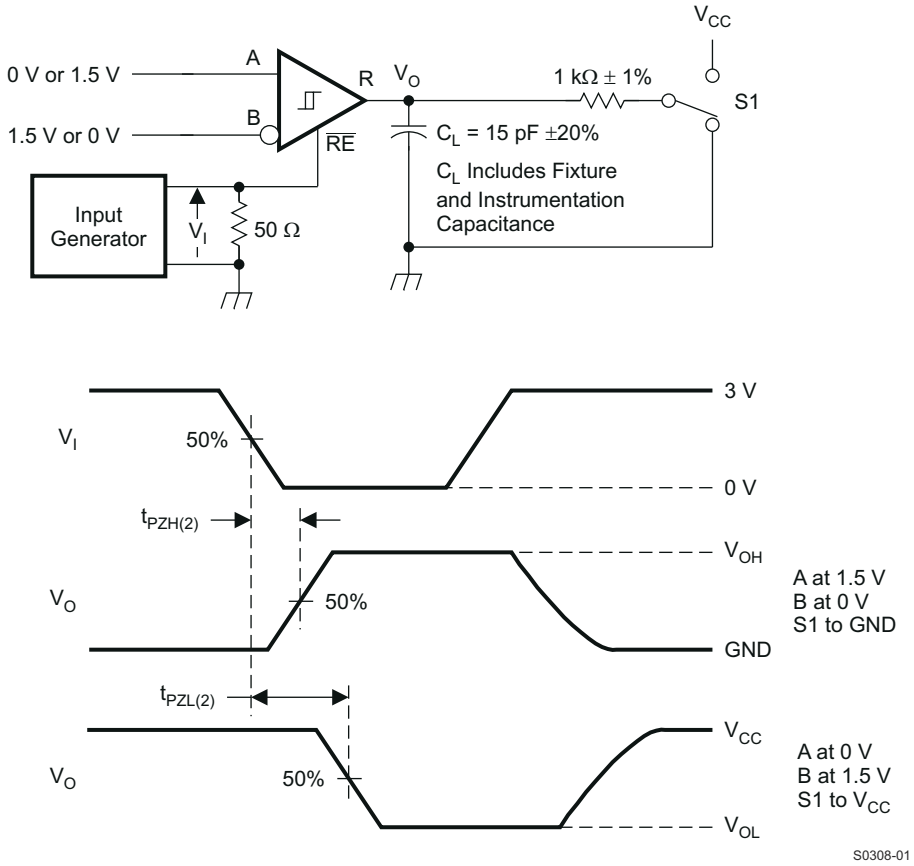


Figure 8-8. Measurement of Receiver Enable Times With Driver Disabled

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9 Detailed Description

9.1 Overview

The SN65HVD17xx family of RS-485 transceivers are designed to operate up to 115 kbps (HVD1785 and HVD1791), 1 Mbps (HVD1786 and HVD1792), or 10 Mbps (HVD1787 or HVD1793) and to withstand DC overvoltage faults on the bus interface pins. This helps to protect the devices against damages resulting from direct shorts to power supplies, cable mis-wirings, connector failures, or other common faults.

The SN65HVD178x devices are half-duplex, and thus have the transmitter and receiver bus interfaces connected together internally. The SN65HVD179x family leaves these two interfaces separate, allowing for full-duplex communication. The low receiver loading allows for up to 256 nodes to share a common RS-485 bus. The devices feature a wide common-mode range as well as fail-safe receivers, which ensure a stable logic-level output during bus open, short, or idle conditions.

9.2 Functional Block Diagram

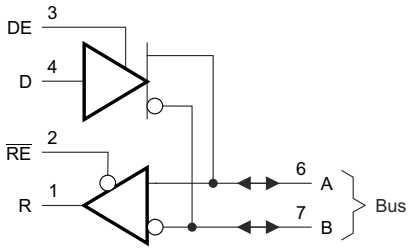


Figure 9-1. Half-Duplex Transceiver

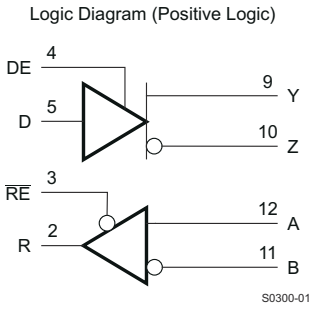


Figure 9-2. Full Duplex Transceiver

9.3 Feature Description

9.3.1 Hot-Plugging

These devices are designed to operate in hot swap or hot pluggable applications. Key features for hot-pluggable applications are power-up, power-down glitch free operation, default disabled input/output pins, and receiver failsafe. As shown in Figure 7-1, an internal Power-On Reset circuit keeps the driver outputs in a high-impedance state until the supply voltage has reached a level at which the device will reliably operate. This ensures that no spurious transitions (glitches) will occur on the bus pin outputs as the power supply turns on or turns off.

As shown in *Section 9.4*, the *ENABLE* inputs have the feature of default disable on both the driver enable and receiver enable. This ensures that the device will neither drive the bus nor report data on the R pin until the associated controller actively drives the enable pins.

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9.3.2 Receiver Failsafe

The differential receiver is *failsafe* to invalid bus states caused by:

- open bus conditions such as a disconnected connector,
- shorted bus conditions such as cable damage shorting the twisted-pair together,
- or idle bus conditions that occur when no driver on the bus is actively driving.

In any of these cases, the differential receiver outputs a failsafe logic High state, so that the output of the receiver is not indeterminate.

In the HVD17xx family of RS-485 devices, receiver failsafe is accomplished by offsetting the receiver thresholds so that the “input indeterminate” range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a High when the differential input V_{ID} is more positive than 200 mV, and must output a Low when the V_{ID} is more negative than -200 mV. The HVD17xx receiver parameters which determine the failsafe performance are V_{IT+} and V_{IT-} and V_{HYS}. In the *Electrical Characteristics* table, V_{IT-} has a typical value of –150 mV and a minimum (most negative) value of -200 mV, so differential signals more negative than -200 mV will always cause a Low receiver output. Similarly, differential signals more positive than 200 mV will always cause a High receiver output, because the typical value of V_{IT+} is -100mV, and V_{IT+} is never more positive than -10 mV under any conditions of temperature, supply voltage, or common-mode offset.

When the differential input signal is close to zero, it will still be above the V_{IT+} threshold, and the receiver output will be High. Only when the differential input is more negative than V_{IT-} will the receiver output transition to a Low state. So, the noise immunity of the receiver inputs during a bus fault condition includes the receiver hysteresis value V_{HYS} (the separation between V_{IT+} and V_{IT-}) as well as the value of V_{IT+}.

For the HVD17xx devices, the typical noise immunity is typically about 150 mV, which is the negative noise level needed to exceed the V_{IT-} threshold (V_{IT-} TYP = –150 mV). In the worst case, the failsafe noise immunity is never less than 40 mV, which is set by the maximum positive threshold (V_{IT+} MAX = –10 mV) plus the minimum hysteresis voltage (V_{HYS} MIN = 30 mV).

9.3.3 70-V Fault-Protection

The SN65HVD17xx family of RS-485 devices is designed to survive bus pin faults up to ±70V. The devices designed for fast signaling rate (10 Mbps) will not survive a bus pin fault with a direct short to voltages above 30V when:

1. the device is powered on AND

2a. the driver is enabled (DE=HIGH) AND D=HIGH AND the bus fault is applied to the A pin OR

2b. the driver is enabled (DE=HIGH) AND D=LOW AND the bus fault is applied to the B pin

Under other conditions, the device will survive shorts to bus pin faults up to 70V. Table 9-1 summarizes the conditions under which the device may be damaged, and the conditions under which the device will not be damaged.

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Table 9-1. Device Conditions

POWER	DE	D	A	B	RESULTS
OFF	X	X	-70V < V_A < 70V	-70V < V_B < 70V	Device survives
ON	LO	X	-70V < V_A < 70V	-70V < V_B < 70V	Device survives
ON	HI	L	-70V < V_A < 70V	-70V < V_B < 30V	Device survives
ON	HI	L	-70V < V_A < 70V	30V < V_B	Damage may occur
ON	HI	H	-70V < V_A < 30V	-70V < V_B < 30V	Device survives
ON	HI	H	30V < V_A	-70V < V_B < 30V	Damage may occur

9.3.4 Additional Options

The SN65HVD17xx family also has options for J1708 applications, for always-enabled full-duplex versions (industry-standard SN65LBC179 footprint) and for inverting-polarity versions, which allow users to correct a reversal of the bus wires without re-wiring. Contact your local Texas Instruments representative for information on these options.

Table 9-2. SN65HVD17xx Options for J1708 Applications

PART NUMBER	SN65HVD17xx		
FOOTPRINT/FUNCTION	SLOW	MEDIUM	FAST
Half-duplex (176 pinout)	85	86	87
Full-duplex no enables (179 pinout)	88	89	90
Full-duplex with enables (180 pinout)	91	92	93
Half-duplex with cable invert	94	95	96
Full-duplex with cable invert and enables	97	98	99
J1708	08	09	10

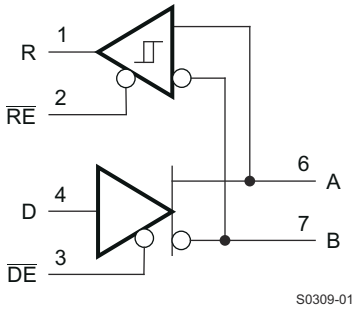


Figure 9-3. SN65HVD1708E Transceiver for J1708 Applications

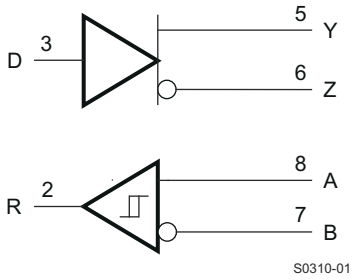


Figure 9-4. SN65HVD17xx Always-Enabled Driver Receiver

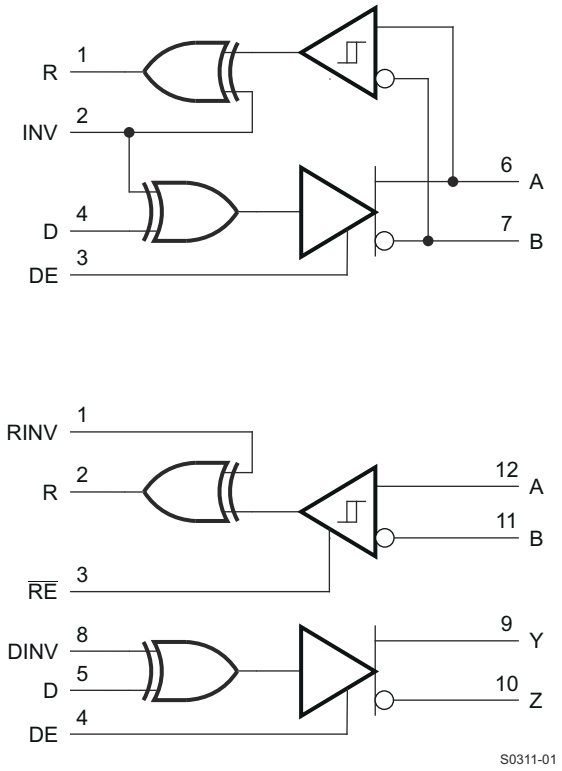


Figure 9-5. SN65HVD17xx Options With Inverting Feature to Correct for Miswired Cables

9.4 Device Functional Modes

Table 9-3. Driver Function Table

INPUT	ENABLE	OUTPUTS		
D	DE	A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

Table 9-4. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	
$V_{ID} = V_A - V_B$	RE	R	
$V_{IT+} < V_{ID}$	L	H	Receive valid bus high
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

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10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN65HVD17xx family consists of both half-duplex and full-duplex transceivers that can be used for asynchronous data communication. Half-duplex implementations require one signaling pair (two wires), while full-duplex implementations require two signaling pairs (four wires). The driver and receiver enable pins of the SN65HVD17xx family allow for control over the direction of data flow. Since it is common for multiple transceivers to share a common communications bus, care should be taken at the system level to ensure that only one driver is enabled at a time. This avoids bus contention, a fault condition in which multiple drivers attempt to send data at the same time.

10.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

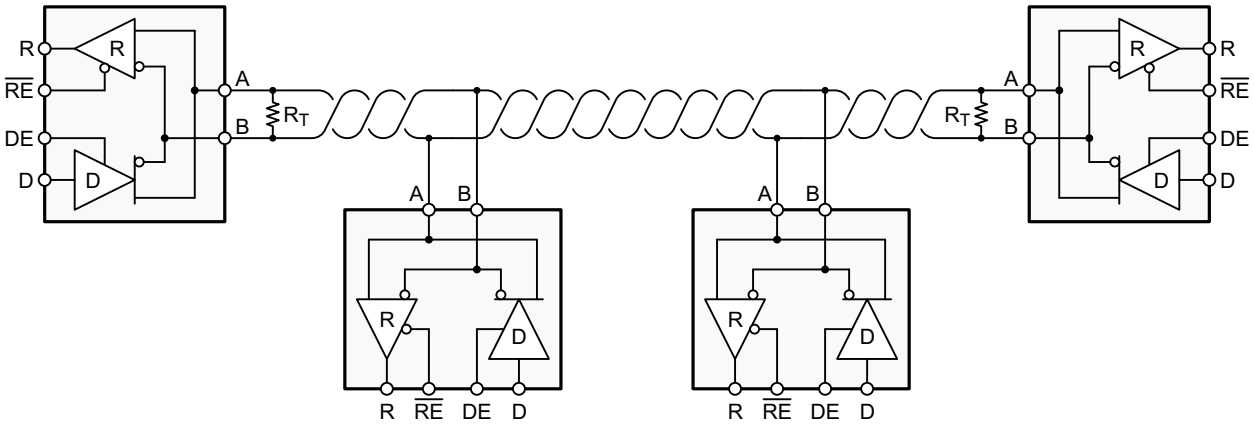


Figure 10-1. Typical RS-485 Network With Half-duplex Transceivers

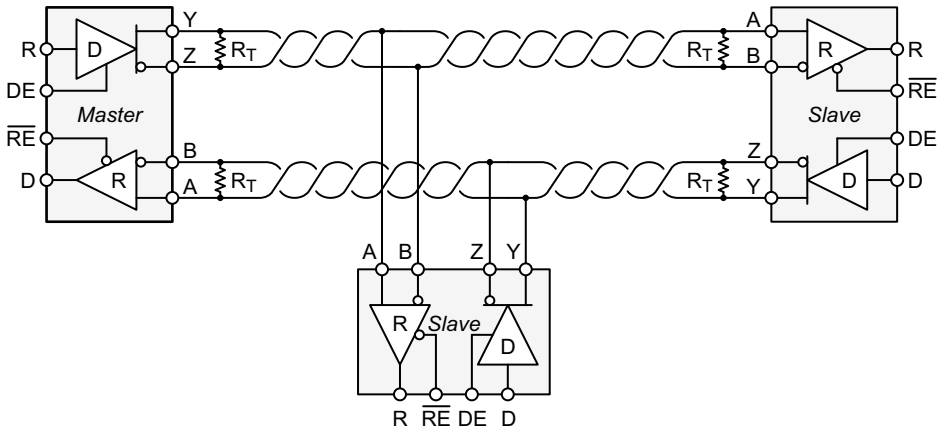


Figure 10-2. Typical RS-485 Network With Full-duplex Transceivers

10.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

10.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the short the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

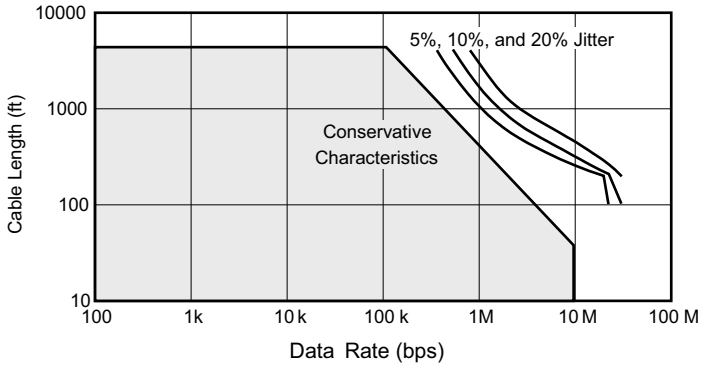


Figure 10-3. Cable Length vs Data Rate Characteristic

Even higher data rates are achievable (for example, 10 Mbps for the SN65HVD1787 and SN65HVD1793) in cases where the interconnect is short enough (or has suitably low attenuation at signal frequencies) to not degrade the data.

10.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in Equation 1.

$$L_{stub} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of *c*

10.2.1.3 Receiver Failsafe

The differential receiver of the SN75HVD17xx family is *failsafe* to invalid bus states caused by:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

n any of these cases, the differential receiver will output a failsafe logic high state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the “input indeterminate” range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input V_{ID} is more positive than +200 mV, and must output a low

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when VID is more negative than -200 mV. The receiver parameters which determine the failsafe performance are $V_{IT(+)}$ and $V_{IT(-)}$. As shown in the Electrical Characteristics table, differential signals more negative than -200 mV will always cause a low receiver output, and differential signals more positive than +200 mV will always cause a high receiver output.

When the differential input signal is close to zero, it is still above the maximum $V_{IT(+)}$ threshold of -10 mV, and the receiver output will be high.

10.2.2 Detailed Design Procedure

Although the SN65HVD17xx family is internally protected against human-body-model ESD strikes up to 16 kV, additional protection against higher-energy transients can be provided at the application level by implementing external protection devices.

10.2.3 Application Curve

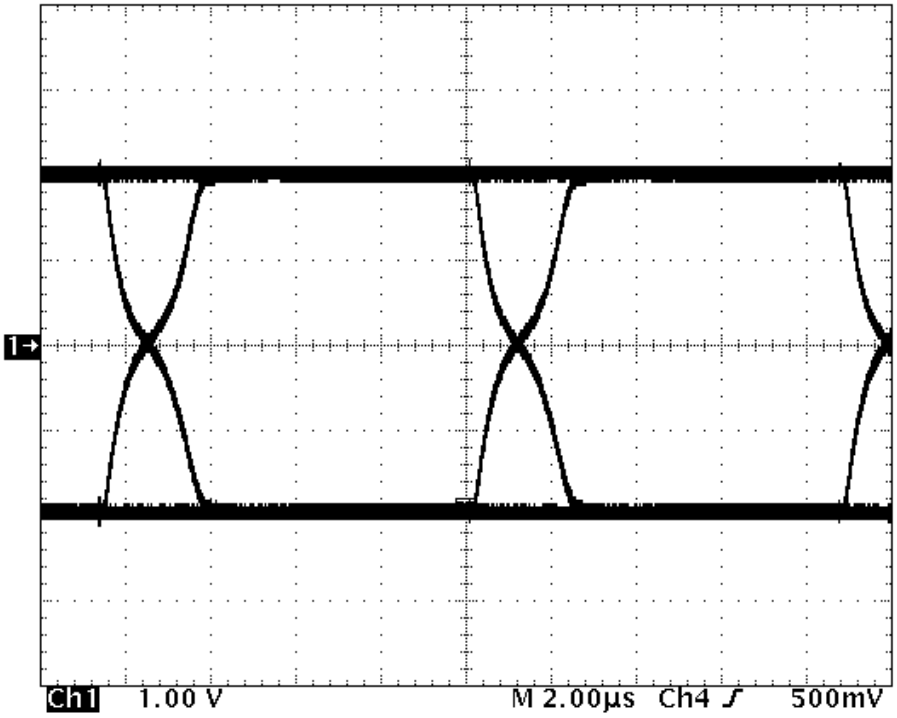


Figure 10-4. SN65HVD1785 Differential Output at 115 kbps

11 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100-nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

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12 Layout

12.1 Layout Guidelines

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100-nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

1. Place the protection circuitry close to the bus connector to prevent noise transients from entering the board.
2. Use V_{CC} and ground planes to provide low-inductance power distribution. Note that high-frequency currents tend to follow the path of least inductance and not the path of least resistance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100-nF-to-220-nF bypass capacitors as close as possible to the V_{CC} pins of transceiver, UART, or controller ICs on the board.
5. Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
6. Use 1-kΩ-to-10-kΩ pullup and pulldown resistors for enable lines to limit noise currents in these lines during transient events.
7. Insert series pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus terminals. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
8. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.

12.2 Layout Example

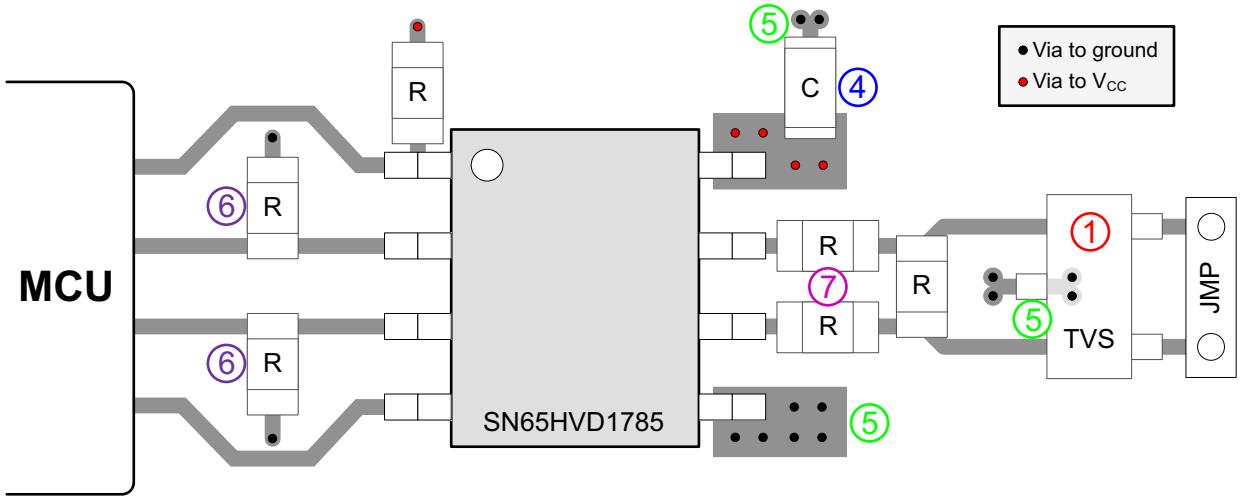


Figure 12-1. Layout Example (Half-Duplex Transceiver)

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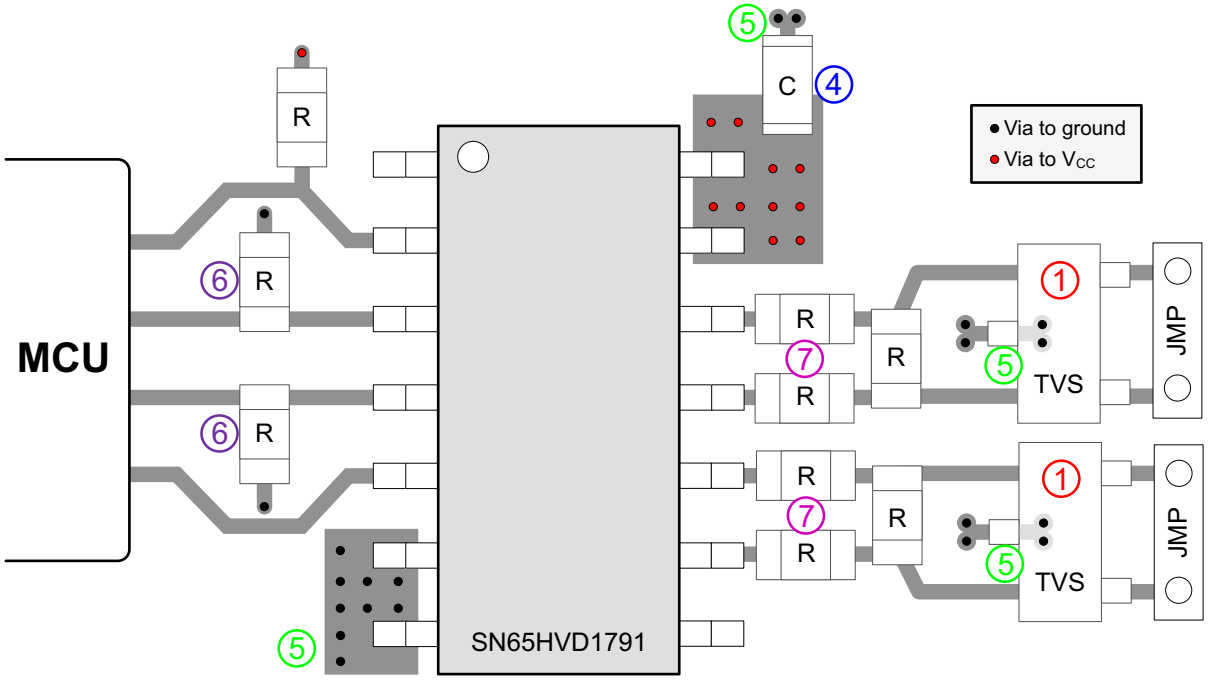


Figure 12-2. Layout Example (Full-Duplex Transceiver)

13 Device and Documentation Support

13.1 Documentation Support

For related documentation see the following:

SN65HVD1781, *Fault-Protected RS-485 Transceivers With 3.3-V to 5-V Operation*, (SLLS877)

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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13.4 Trademarks

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All trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65HVD1785D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1785
SN65HVD1785D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1785
SN65HVD1785D.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1785
SN65HVD1785DG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1785
SN65HVD1785DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1785
SN65HVD1785DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1785
SN65HVD1785DR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1785
SN65HVD1785DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1785
SN65HVD1785P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	65HVD1785
SN65HVD1785P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	65HVD1785
SN65HVD1785P.B	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	65HVD1785
SN65HVD1786D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1786
SN65HVD1786D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1786
SN65HVD1786D.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1786
SN65HVD1786DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1786
SN65HVD1786DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1786
SN65HVD1786DR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1786
SN65HVD1786DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1786
SN65HVD1786P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	65HVD1786
SN65HVD1786P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	65HVD1786
SN65HVD1786P.B	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	65HVD1786
SN65HVD1787D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1787
SN65HVD1787D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1787
SN65HVD1787DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1787
SN65HVD1787DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1787
SN65HVD1787DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1787
SN65HVD1787DRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1787
SN65HVD1791D	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1791
SN65HVD1791D.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1791

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65HVD1791DG4	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1791
SN65HVD1791DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1791
SN65HVD1791DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1791
SN65HVD1791DRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1791
SN65HVD1791DRG4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1791
SN65HVD1792D	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1792
SN65HVD1792D.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1792
SN65HVD1792DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1792
SN65HVD1792DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1792
SN65HVD1792DRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1792
SN65HVD1792DRG4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1792
SN65HVD1793D	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1793
SN65HVD1793D.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1793
SN65HVD1793DG4	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1793
SN65HVD1793DG4.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1793
SN65HVD1793DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1793
SN65HVD1793DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	VP1793

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN65HVD1792 :

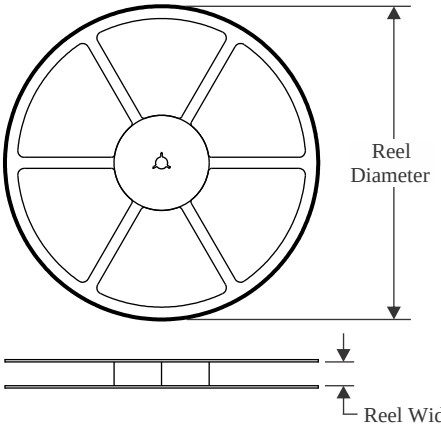
- Enhanced Product : SN65HVD1792-EP

NOTE: Qualified Version Definitions:

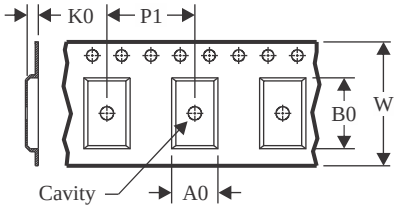
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

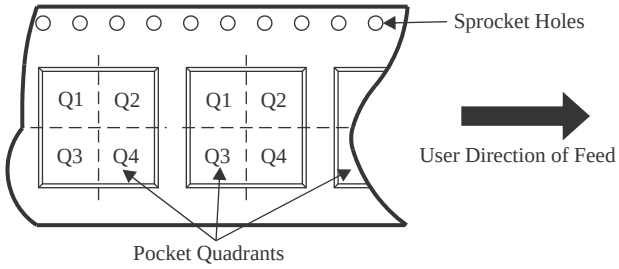


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

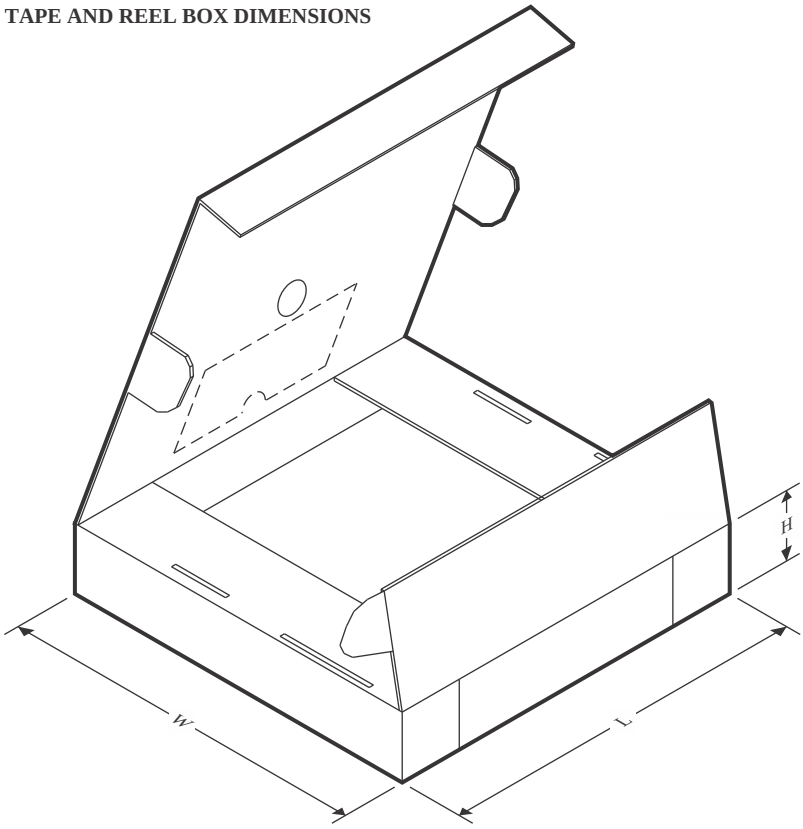
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD1785DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD1787DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD1787DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD1791DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65HVD1791DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65HVD1792DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65HVD1792DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65HVD1793DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

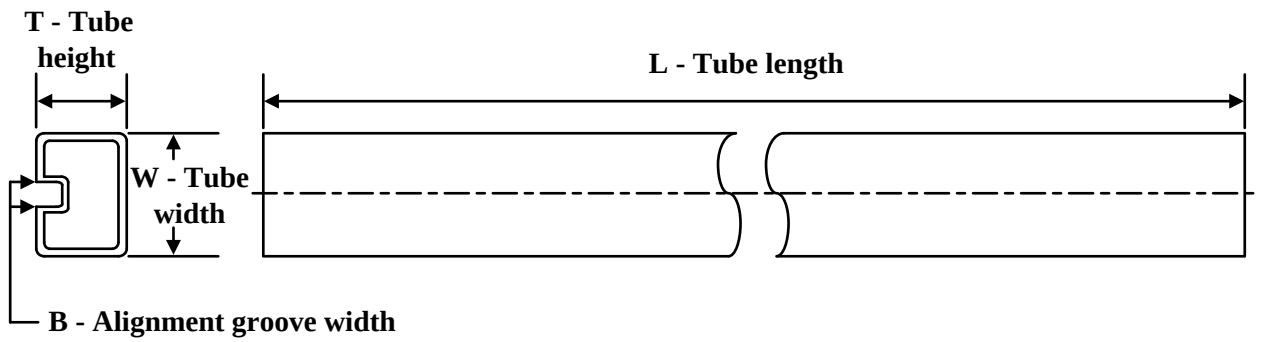
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

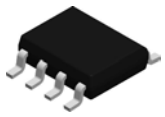
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD1785DR	SOIC	D	8	2500	353.0	353.0	32.0
SN65HVD1787DR	SOIC	D	8	2500	353.0	353.0	32.0
SN65HVD1787DRG4	SOIC	D	8	2500	353.0	353.0	32.0
SN65HVD1791DR	SOIC	D	14	2500	353.0	353.0	32.0
SN65HVD1791DRG4	SOIC	D	14	2500	353.0	353.0	32.0
SN65HVD1792DR	SOIC	D	14	2500	353.0	353.0	32.0
SN65HVD1792DRG4	SOIC	D	14	2500	353.0	353.0	32.0
SN65HVD1793DR	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65HVD1785D	D	SOIC	8	75	506.6	8	3940	4.32
SN65HVD1785D.A	D	SOIC	8	75	506.6	8	3940	4.32
SN65HVD1785D.B	D	SOIC	8	75	506.6	8	3940	4.32
SN65HVD1785DG4	D	SOIC	8	75	506.6	8	3940	4.32
SN65HVD1785P	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD1785P.A	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD1785P.B	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD1786D	D	SOIC	8	75	506.6	8	3940	4.32
SN65HVD1786D.A	D	SOIC	8	75	506.6	8	3940	4.32
SN65HVD1786D.B	D	SOIC	8	75	506.6	8	3940	4.32
SN65HVD1786P	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD1786P.A	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD1786P.B	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD1787D	D	SOIC	8	75	506.6	8	3940	4.32
SN65HVD1787D.A	D	SOIC	8	75	506.6	8	3940	4.32
SN65HVD1791D	D	SOIC	14	50	506.6	8	3940	4.32
SN65HVD1791D.A	D	SOIC	14	50	506.6	8	3940	4.32
SN65HVD1791DG4	D	SOIC	14	50	506.6	8	3940	4.32
SN65HVD1792D	D	SOIC	14	50	506.6	8	3940	4.32
SN65HVD1792D.A	D	SOIC	14	50	506.6	8	3940	4.32
SN65HVD1793D	D	SOIC	14	50	506.6	8	3940	4.32
SN65HVD1793D.A	D	SOIC	14	50	506.6	8	3940	4.32
SN65HVD1793DG4	D	SOIC	14	50	506.6	8	3940	4.32
SN65HVD1793DG4.A	D	SOIC	14	50	506.6	8	3940	4.32

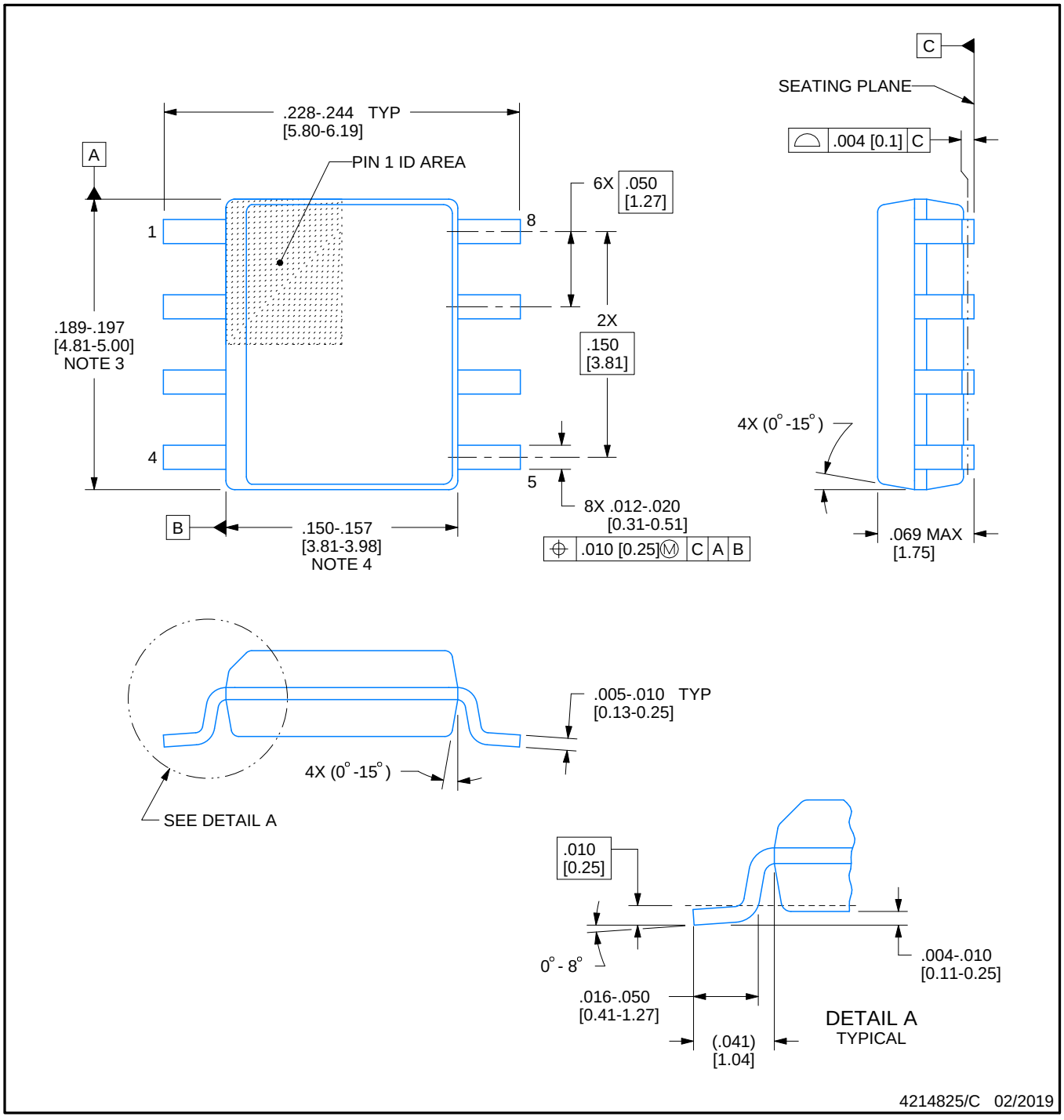


PACKAGE OUTLINE

D0008A

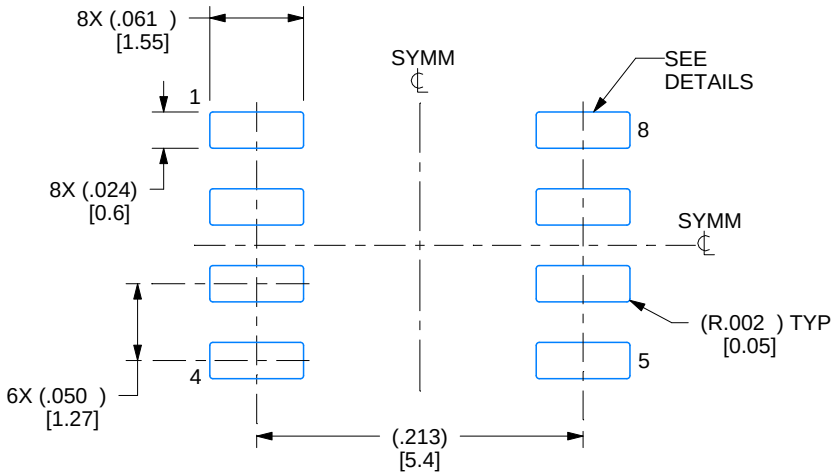
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

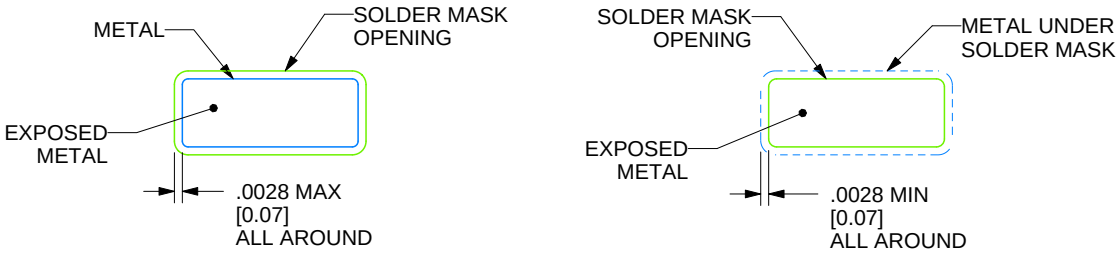


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

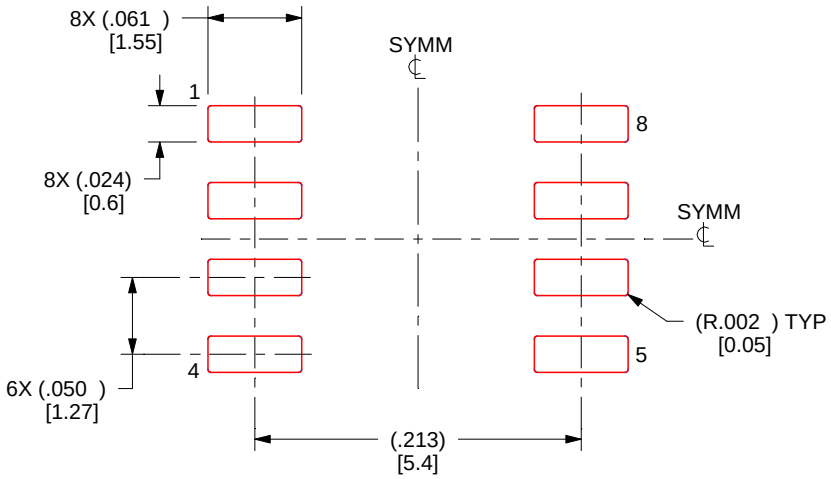
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



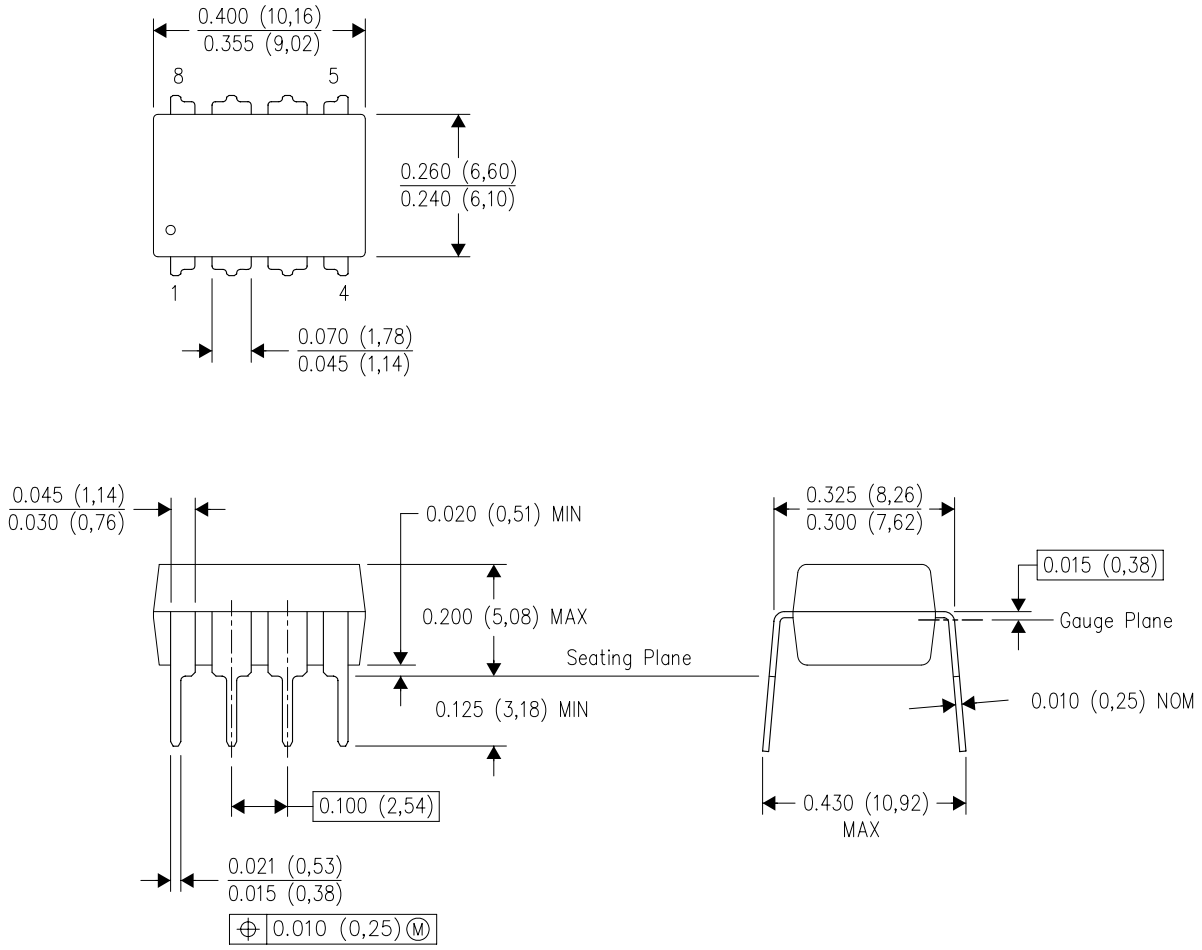
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

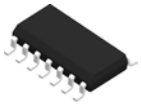
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

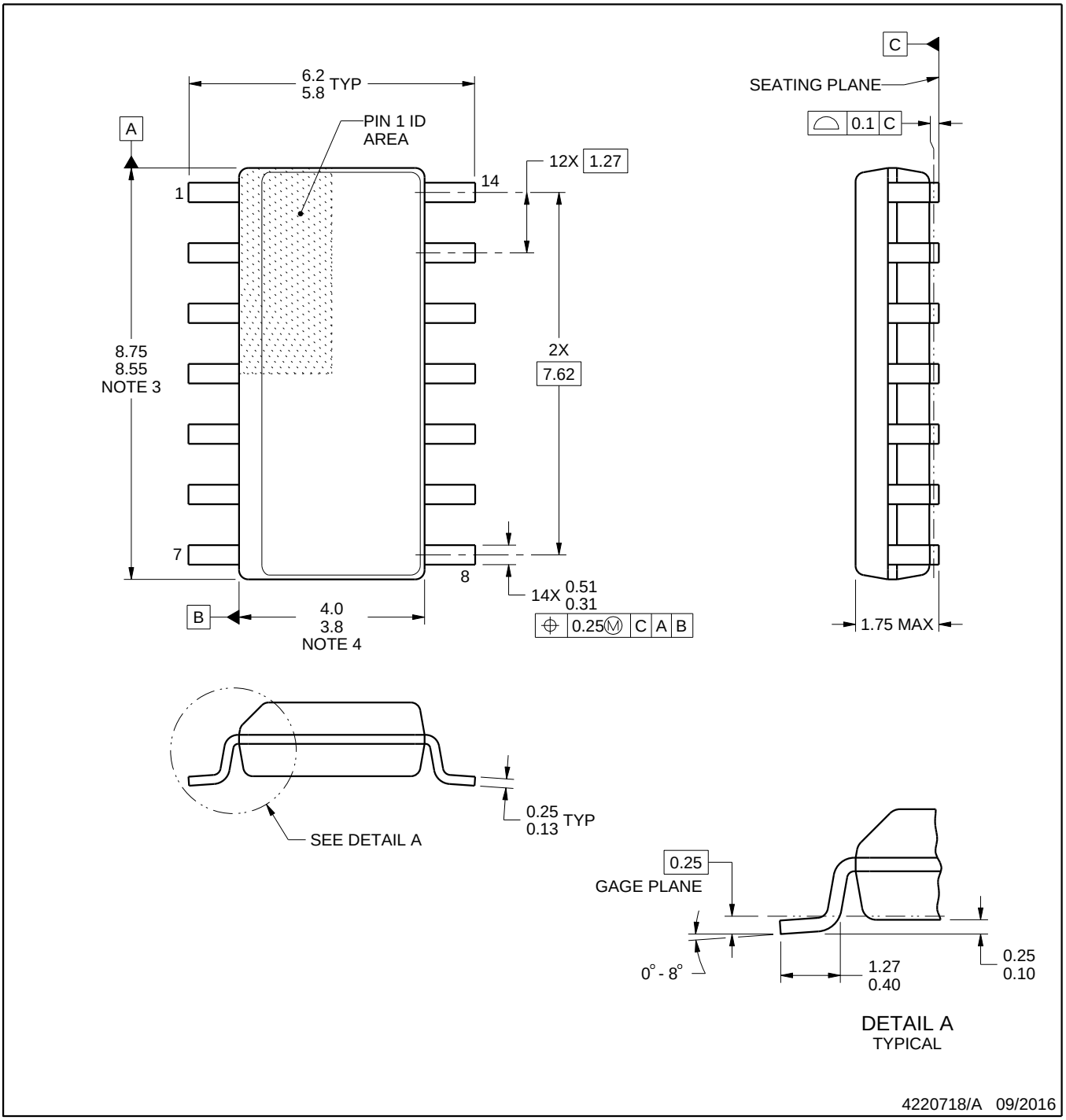


PACKAGE OUTLINE

D0014A

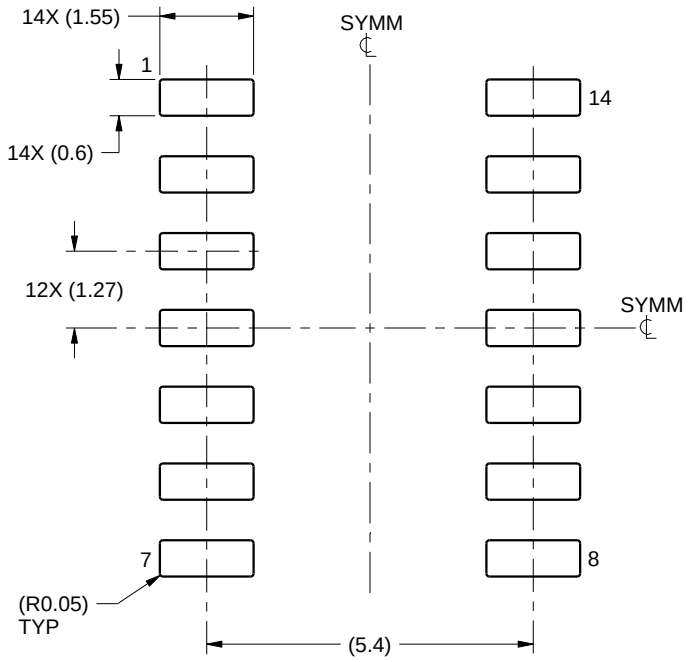
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

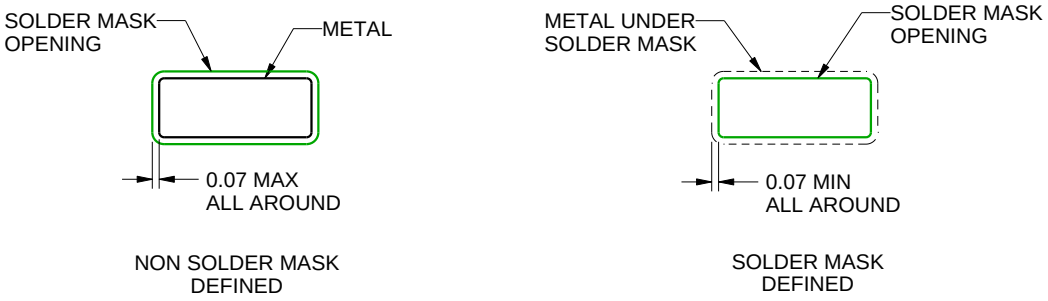


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

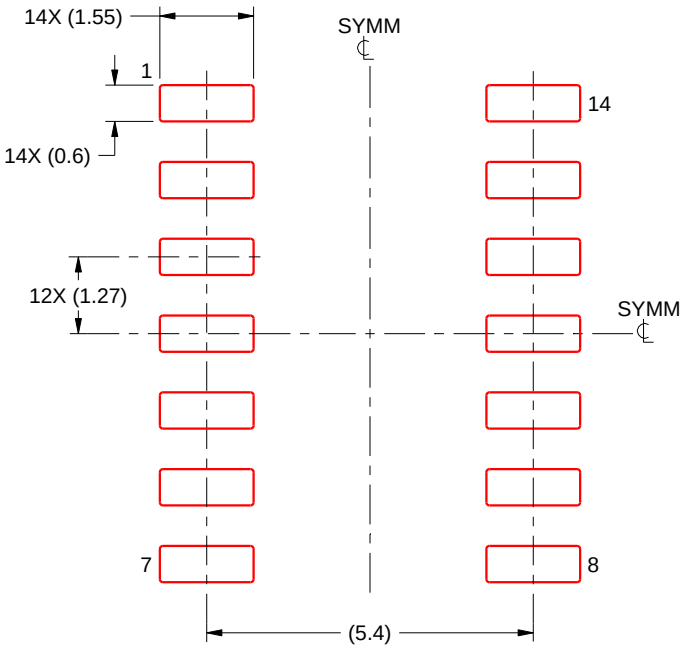
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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