LMC646x Dual and Quad, Micropower, Rail-to-Rail Input/Output, CMOS Operational Amplifiers

1 Features

- Typical values unless otherwise noted
- Ultra low supply current; 20µA/amplifier
- Specified characteristics at 3V and 5V
- Rail-to-rail input common-mode voltage range
- Rail-to-rail output swing
  - Within 10mV of rail, V_S = 5V and R_L = 25kΩ
- Low input current: 150fA
- Low input offset voltage: 0.25mV

2 Applications

- Battery-operated circuits
- Transducer interface circuits
- Portable-communication devices
- Medical applications
- Battery monitoring

3 Description

The LMC6462 and LMC6464 (LMC646x) are micropower versions of the popular LMC6482 and LMC6484, combining a rail-to-rail input and output range with very low power consumption.

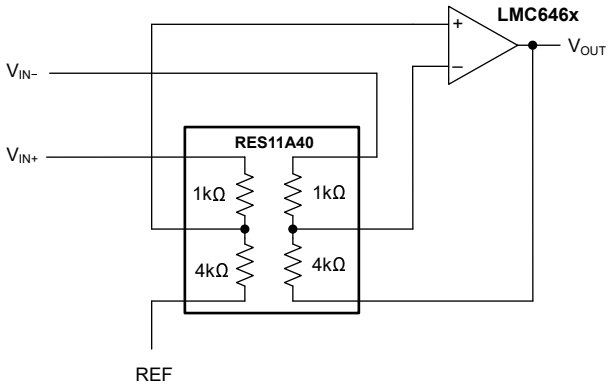
The LMC646x provide an input common-mode voltage range that exceeds both rails. The rail-to-rail output swing of the amplifiers, specified for loads down to 25kΩ, provides maximum dynamic signal range. This rail-to-rail performance of the amplifiers, combined with a high voltage gain, makes these device unique among rail-to-rail amplifiers. The LMC646x are an excellent upgrade for circuits using limited common-mode range amplifiers.

The LMC646x, with specifications at 3V and 5V, is an excellent choice for low-voltage applications. A quiescent power consumption of 60µW per amplifier (at V_S = 3V) can extend the useful life of battery-operated systems. The 150fA input current, low offset voltage of 0.25mV, and 85dB CMRR maintain accuracy in battery-powered systems.

Device Information

PART NUMBER	CHANNEL COUNT	PACKAGE(1)
LMC6462	Dual	D (SOIC, 8)
		P (PDIP, 8)
LMC6464	Quad	D (SOIC, 14)
		N (PDIP, 14)

(1) For more information, see Section 10.



Difference Amplifier With RES11A

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4 Pin Configuration and Functions

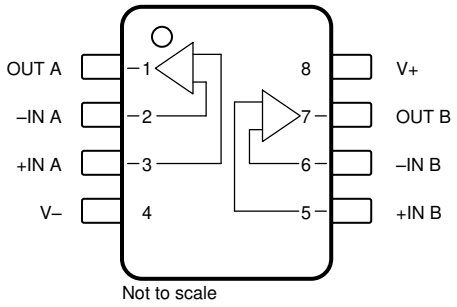

Figure 4-1. LMC6462: D Package, 8-Pin SOIC, and P Package, 8-Pin PDIP (Top View)

Table 4-1. Pin Functions: LMC6462

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN A	2	Input	Inverting input channel A
–IN B	6	Input	Inverting input channel B
+IN A	3	Input	Noninverting input channel A
+IN B	5	Input	Noninverting input channel B
OUT A	1	Output	Output channel A
OUT B	7	Output	Output channel B
V–	4	Power	Negative supply
V+	8	Power	Positive supply

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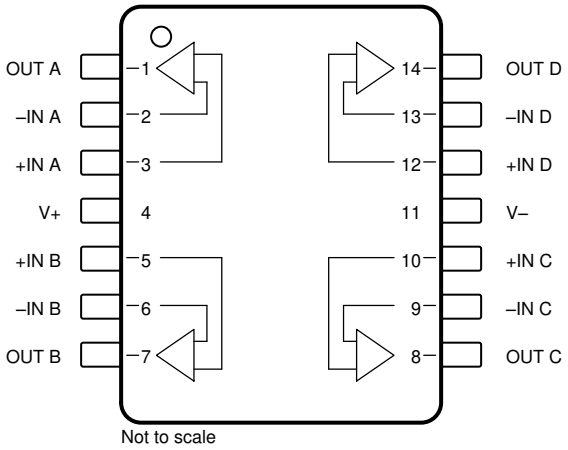

Figure 4-2. LMC6464: D Package, 14-Pin SOIC, and N Package, 14-Pin PDIP (Top View)

Table 4-2. Pin Functions: LMC6464

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN A	2	Input	Inverting input channel A
–IN B	6	Input	Inverting input channel B
–IN C	9	Input	Inverting input channel C
–IN D	13	Input	Inverting input channel D
+IN A	3	Input	Noninverting input channel A
+IN B	5	Input	Noninverting input channel B
+IN C	10	Input	Noninverting input channel C
+IN D	12	Input	Noninverting input channel D
OUT A	1	Output	Output channel A
OUT B	7	Output	Output channel B
OUT C	8	Output	Output channel C
OUT D	14	Output	Output channel D
V–	11	Power	Negative supply
V+	4	Power	Positive supply

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
	Differential input voltage		±Supply voltage	V
V_S	Supply voltage, V_S = (V+) – (V–)		16	V
	Voltage at input/output pin	(V–) – 0.3	(V+) + 0.3	V
	Current at input pin(3)		±5	mA
	Current at output pin(4) (5)		±30	mA
	Current at power supply pin		40	mA
T_J	Junction temperature(6)		150	°C
T_{stg}	Storage temperature	–65	150	°C
	Lead temperature (soldering, 10s)		260	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.
(4) Applies to both single supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30mA over long term can adversely affect reliability.
(5) Do not short circuit output to V+, when V+ is greater than 13V or reliability is adversely affected.
(6) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly into a PCB.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	3		15.5	V
T_J	Junction temperature	–40		85	°C

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5.4 Thermal Information for LMC6462

THERMAL METRIC[1]		LMC6462		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193	115	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	52.0	53.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.9	39.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.8	19.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.1	38.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Thermal Information for LMC6464

THERMAL METRIC[1]		LMC6464		UNIT
		D (SOIC)	NFF (PDIP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	126	81	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	34.6	31.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.3	26.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.7	9.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33.7	25.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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5.6 Electrical Characteristics for V_S = ±2.25V or V_S = 5V

at $T_A = T_J$ = 25°C, V+ = 5V, V– = 0V, $V_{CM} = V_{OUT}$ = V+ / 2, and R_L > 1MΩ connected to V+ / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	LMC646xA			±0.25	±0.50	mV
			T_J = –40°C to +85°C			±1.2	
		LMC646xB			±0.25	±3	
			T_J = –40°C to +85°C			±3.7	
dV_{OS}/dT	Input offset voltage drift		T_J = –40°C to +85°C		1		µV/°C
PSRR	Power-supply rejection ratio	Positive 5V ≤ V+ ≤ 15V	LMC646xA	70	85		dB
			LMC646xA, T_J = –40°C to +85°C	67			
			LMC646xB	65	85		
			LMC646xB, T_J = –40°C to +85°C	62			
		Negative V+ = 0V, –15V ≤ V– ≤ –5V	LMC646xA	70	85		
			LMC646xA, T_J = –40°C to +85°C	67			
			LMC646xB	65	85		
			LMC646xB, T_J = –40°C to +85°C	62			
INPUT BIAS CURRENT							
I_B	Input bias current(1)				±0.15		pA
		T_J = –40°C to +85°C				±10	
I_{OS}	Input offset current(1)				±0.075		pA
		T_J = –40°C to +85°C				±5	
NOISE							
e_n	Input voltage noise density	f = 1kHz, V_{CM} = 1V			80		nV/√Hz
i_n	Input current noise density	f = 1kHz			30		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage	To positive rail V+ = 5V, CMRR ≥ 50dB		5.25	5.30		V
			T_J = –40°C to +85°C	5.00			
		To negative rail V+ = 5V, CMRR ≥ 50dB			–0.20	–0.10	
			T_J = –40°C to +85°C			0.00	
		To positive rail V+ = 5V, CMRR ≥ 50dB		15.25	15.30		
			T_J = –40°C to +85°C	15.00			
		To negative rail V+ = 5V, CMRR ≥ 50dB			–0.20	–0.15	
			T_J = –40°C to +85°C			0.00	
CMRR	Common-mode rejection ratio	V+ = 15V 0V ≤ V_{CM} ≤ 15V	LMC646xA	70	85		dB
			LMC646xA, T_J = –40°C to +85°C	67			
			LMC646xB	65	85		
			LMC646xB, T_J = –40°C to +85°C	62			
		V+ = 5V 0V ≤ V_{CM} ≤ 5V	LMC646xA	70	85		
			LMC646xA, T_J = –40°C to +85°C	67			
			LMC646xB	65	85		
			LMC646xB, T_J = –40°C to +85°C	62			

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5.6 Electrical Characteristics for V_S = ±2.25V or V_S = 5V (continued)

at $T_A = T_J$ = 25°C, V+ = 5V, V– = 0V, $V_{CM} = V_{OUT}$ = V+ / 2, and R_L > 1MΩ connected to V+ / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT IMPEDANCE							
R_{IN}	Input resistance				> 10		TΩ
C_{IN}	Common-mode input capacitance				3		pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	Sourcing, V+ = 15V, 7.5V < V_O < 11.5V, V_{CM} = 7.5V,	R_L = 100kΩ to 7.5V		3000		V/mV
			R_L = 25kΩ to 7.5V		2500		
		Sinking, V_+ = 15V, 3.5V < V_O < 7.5V, V_{CM} = 7.5V,	R_L = 100kΩ to 7.5V		400		
			R_L = 25kΩ to 7.5V		200		
FREQUENCY RESPONSE							
GBW	Gain bandwidth product				50		kHz
SR	Slew rate[2]	V+ = 15V, 10V step, G = 1		15	28		V/ms
			T_J = –40°C to +85°C	8			
G_m	Gain margin				15		dB
	Crosstalk	Dual and quad channel, V+ = 15V, R_L = 100kΩ to 7.5V, f = 1kHz, V_{OUT} = $12V_{PP}$			130		dB

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5.6 Electrical Characteristics for V_S = ±2.25V or V_S = 5V (continued)

at $T_A = T_J$ = 25°C, V+ = 5V, V– = 0V, $V_{CM} = V_{OUT}$ = V+ / 2, and R_L > 1MΩ connected to V+ / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
V_O	Voltage output swing	Positive rail V+ = 5V, R_L = 100kΩ to V+ / 2	LMC646xA	4.990	4.995		V
			LMC646xA, T_J = –40°C to +85°C	4.980			
			LMC646xB	4.950	4.995		
			LMC646xB, T_J = –40°C to +85°C	4.925			
		Negative rail V+ = 5V, R_L = 100kΩ to V+ / 2	LMC646xA		0.005	0.010	
			LMC646xA, T_J = –40°C to +85°C			0.020	
			LMC646xB		0.005	0.050	
			LMC646xB, T_J = –40°C to +85°C			0.075	
		Positive rail V+ = 5V, R_L = 25kΩ to V+ / 2	LMC646xA	4.975	4.990		
			LMC646xA, T_J = –40°C to +85°C	4.965			
			LMC646xB	4.950	4.990		
			LMC646xB, T_J = –40°C to +85°C	4.850			
		Negative rail V+ = 5V, R_L = 25kΩ to V+ / 2	LMC646xA		0.01	0.02	
			LMC646xA, T_J = –40°C to +85°C			0.035	
			LMC646xB		0.01	0.050	
			LMC646xB, T_J = –40°C to +85°C			0.150	
		Positive rail V+ = 15V, R_L = 100kΩ to V+ / 2	LMC646xA	14.975	14.990		
			LMC646xA, T_J = –40°C to +85°C	14.965			
			LMC646xB	14.950	14.990		
			LMC646xB, T_J = –40°C to +85°C	14.925			
		Negative rail V+ = 15V, R_L = 100kΩ to V+ / 2	LMC646xA		0.01	0.025	
			LMC646xA, T_J = –40°C to +85°C			0.035	
			LMC646xB		0.01	0.050	
			LMC646xB, T_J = –40°C to +85°C			0.075	
		Positive rail V+ = 15V, R_L = 25kΩ to V+ / 2	LMC646xA	14.900	14.965		
			LMC646xA, T_J = –40°C to +85°C	14.850			
			LMC646xB	14.850	14.965		
			LMC646xB, T_J = –40°C to +85°C	14.800			
		Negative rail V+ = 15V, R_L = 25kΩ to V+ / 2	LMC646xA		0.025	0.050	
			LMC646xA, T_J = –40°C to +85°C			0.150	
			LMC646xB		0.025	0.100	
			LMC646xB, T_J = –40°C to +85°C			0.200	

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5.6 Electrical Characteristics for V_S = ±2.25V or V_S = 5V (continued)

at $T_A = T_J$ = 25°C, V+ = 5V, V– = 0V, $V_{CM} = V_{OUT}$ = V+ / 2, and R_L > 1MΩ connected to V+ / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{SC}	Short-circuit current	Sourcing V_{OUT} = 0V		19	27		mA
			T_J = –40°C to +85°C	15			
		Sinking V_{OUT} = 5V		22	27		
			T_J = –40°C to +85°C	17			
		Sourcing V+ = 15V, V_{OUT} = 0V		24	38		
			T_J = –40°C to +85°C	17			
		Sinking V+ = 15V, V_{OUT} = 12V(3)		28	38		
			T_J = –40°C to +85°C	22			
POWER SUPPLY							
I_Q	Quiescent current	V_{OUT} = V+ / 2	LMC6462		40	55	µA
			LMC6462, T_J = –40°C to +85°C			70	
			LMC6464		80	110	
			LMC6464, T_J = –40°C to +85°C			140	
		V+ = 15V, V_{OUT} = V+ / 2	LMC6462		50	60	
			LMC6462, T_J = –40°C to +85°C			70	
			LMC6464		90	120	
			LMC6464, T_J = –40°C to +85°C			140	

(1) Specified limits are dictated by tester limitations and not device performance. Actual performance is reflected in the typical value.
(2) Number specified is the slower of either the positive or negative slew rates.
(3) Do not short circuit output to V+, when V+ is greater than 13V or reliability is adversely affected.

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5.7 Electrical Characteristics for V_S = ±1.5V or V_S = 3V

at T_A = 25°C, V+ = 3V, V– = 0V, V_{CM} = V_{OUT} = V+ / 2, and R_L > 1MΩ connected to V+ / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	LMC646xA			±0.9	±2	mV
			T_A = –40°C to +85°C			±2.7	
		LMC646xB			±0.9	±3	
			T_A = –40°C to +85°C			±3.7	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +85°C			2		µV/°C
PSRR	Power-supply rejection ratio	3V ≤ V+ ≤ 15V		60	80		dB
INPUT BIAS CURRENT							
I_B	Input bias current(1)				±0.15		pA
		T_A = –40°C to +85°C				±10	
I_{OS}	Input offset current(1)				±0.075		pA
		T_A = –40°C to +85°C				±5	
NOISE							
e_n	Input voltage noise density	f = 1kHz, V_{CM} = 1V			80		nV/√Hz
i_n	Input current noise density	f = 1kHz			30		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range	To positive rail V+ = 5V, CMRR ≥ 50dB		3	3		V
		To negative rail V+ = 5V, CMRR ≥ 50dB			–0.1	0	
CMRR	Common-mode rejection ratio	0V ≤ V_{CM} ≤ 3V		60	74		dB
FREQUENCY RESPONSE							
GBW	Gain bandwidth product				50		kHz
SR	Slew rate(2)	G = 1, 2V step			23		V/ms
OUTPUT							
V_O	Voltage output swing	Positive rail R_L = 25kΩ to V+ / 2		2.95	2.9		V
		Negative rail R_L = 25kΩ to V+ / 2			0.1	0.15	V
POWER SUPPLY							
I_Q	Quiescent current	V_{OUT} = V+ / 2	LMC6462		40	55	µA
			LMC6462, T_A = –40°C to +85°C			70	
			LMC6464		80	110	
			LMC6464, T_A = –40°C to +85°C			140	

(1) Specified limits are dictated by tester limitations and not device performance. Actual performance is reflected in the typical value.
(2) Number specified is the slower of either the positive or negative slew rates.

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6 Typical Characteristics

at V_S = 5V, single supply, and T_A = 25°C (unless otherwise specified)

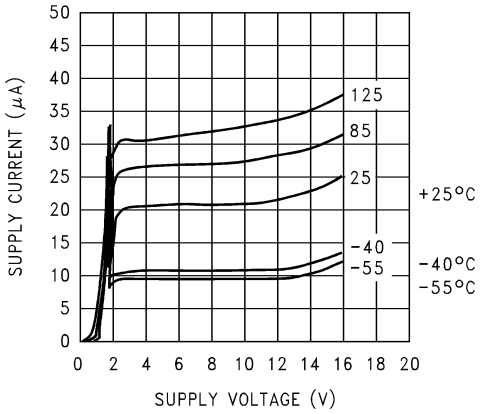

Figure 6-1. Supply Current vs Supply Voltage

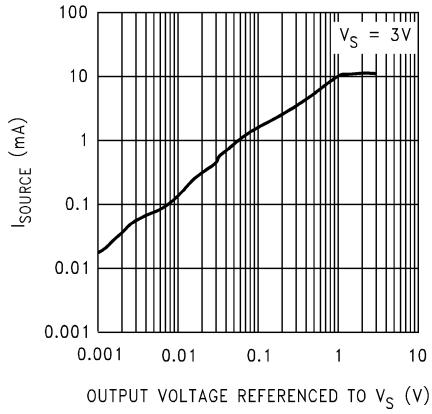

Figure 6-2. Sourcing Current vs Output Voltage

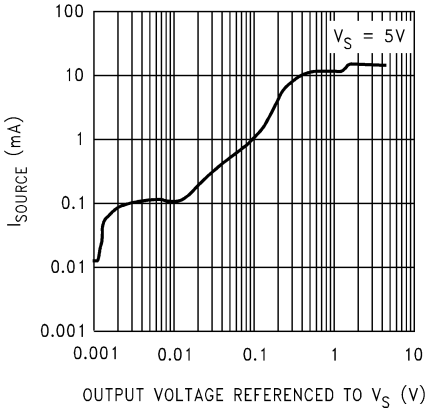

Figure 6-3. Sourcing Current vs Output Voltage

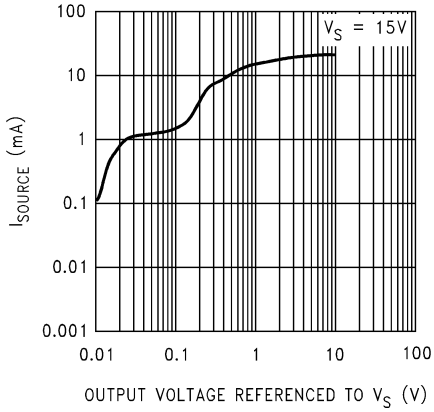

Figure 6-4. Sourcing Current vs Output Voltage

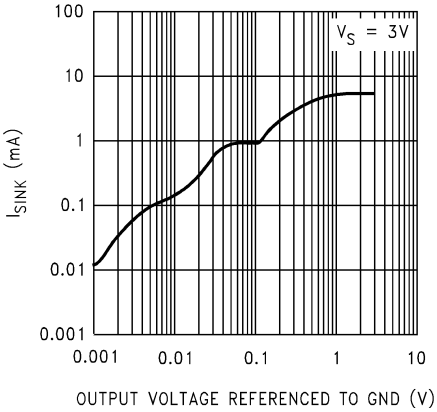

Figure 6-5. Sinking Current vs Output Voltage

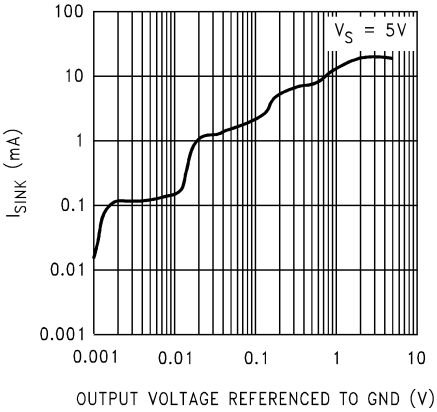

Figure 6-6. Sinking Current vs Output Voltage

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6 Typical Characteristics (continued)

at V_S = 5V, single supply, and T_A = 25°C (unless otherwise specified)

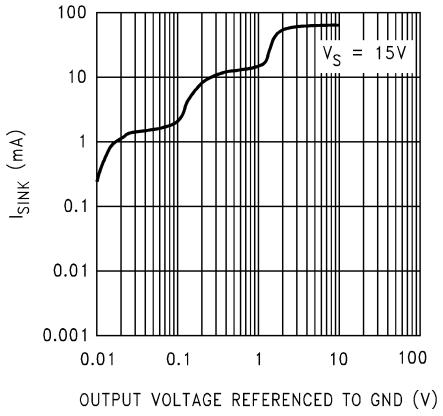


Figure 6-7. Sinking Current vs Output Voltage

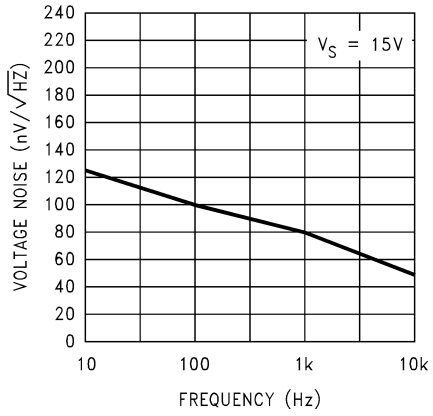
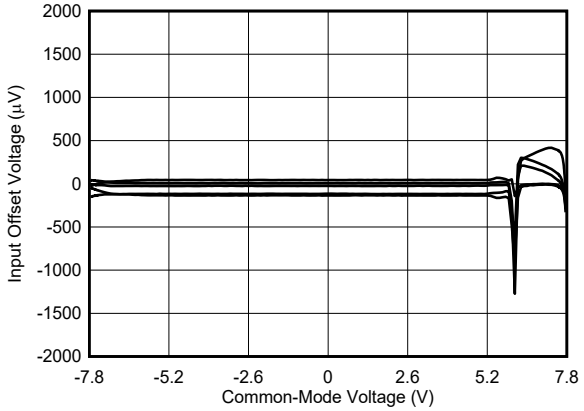
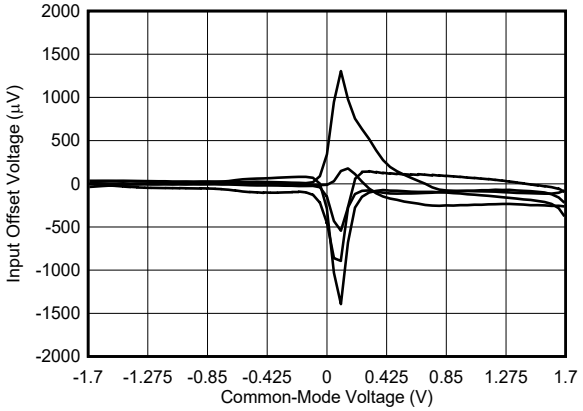


Figure 6-8. Input Voltage Noise vs Frequency



V_S = ±7.5V, 5 typical units

Figure 6-9. Input Offset Voltage vs Common-Mode Voltage



V_S = ±1.5V, 5 typical units

Figure 6-10. Input Offset Voltage vs Common-Mode Voltage

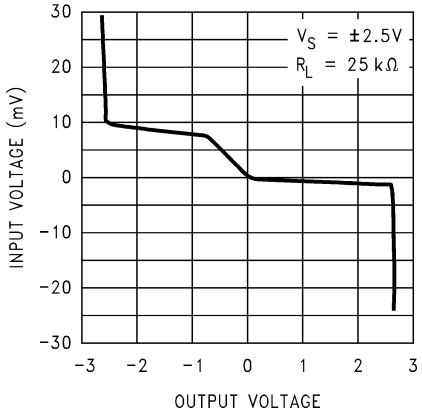


Figure 6-11. Input Voltage vs Output Voltage

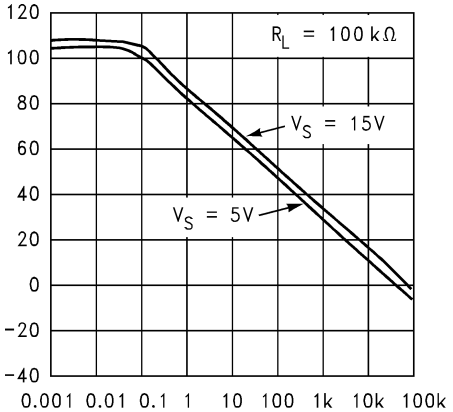


Figure 6-12. Open-Loop Frequency Response

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6 Typical Characteristics (continued)

at V_S = 5V, single supply, and T_A = 25°C (unless otherwise specified)

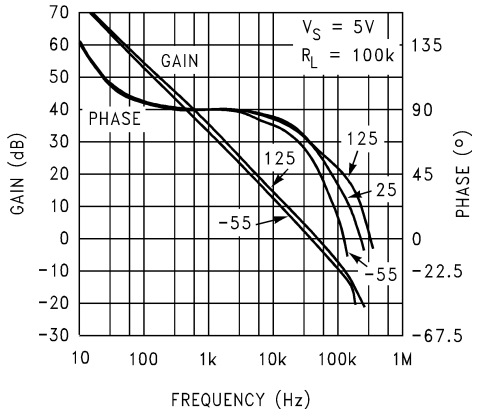

Figure 6-13. Open-Loop Frequency Response vs Temperature

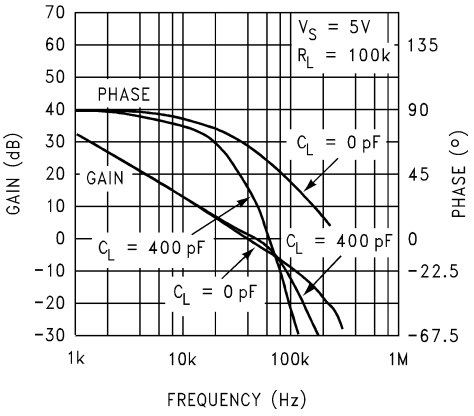

Figure 6-14. Gain and Phase vs Capacitive Load

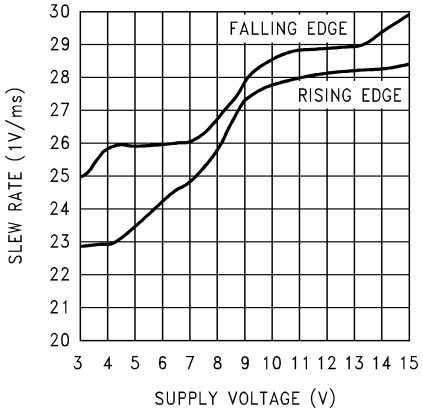

Figure 6-15. Slew Rate vs Supply Voltage

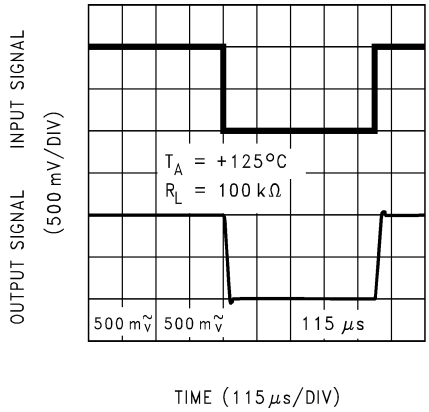

Figure 6-16. Noninverting Large-Signal Pulse Response

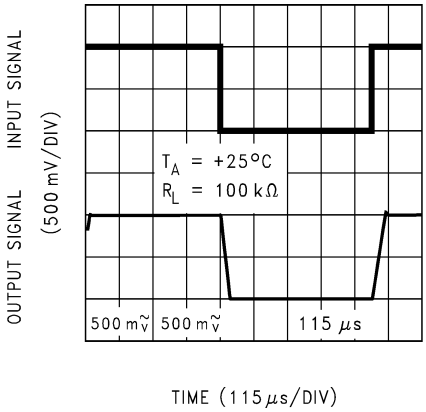

Figure 6-17. Noninverting Large-Signal Pulse Response

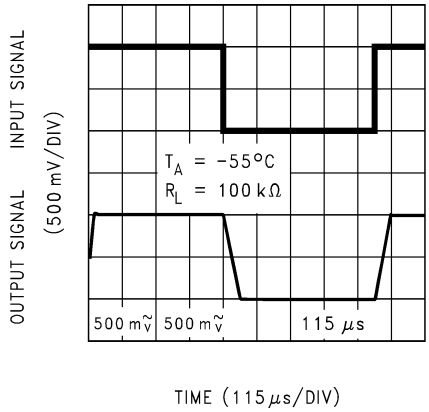

Figure 6-18. Noninverting Large-Signal Pulse Response

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6 Typical Characteristics (continued)

at V_S = 5V, single supply, and T_A = 25°C (unless otherwise specified)

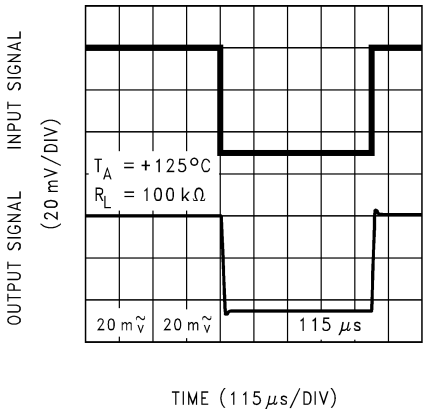

Figure 6-19. Noninverting Small-Signal Pulse Response

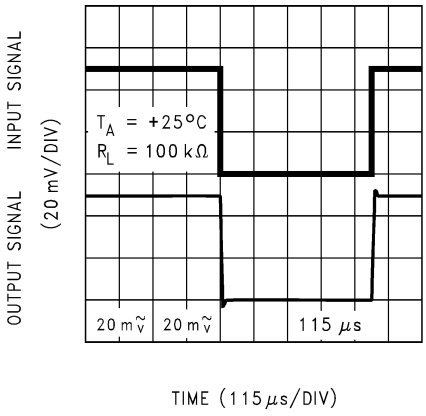

Figure 6-20. Noninverting Small-Signal Pulse Response

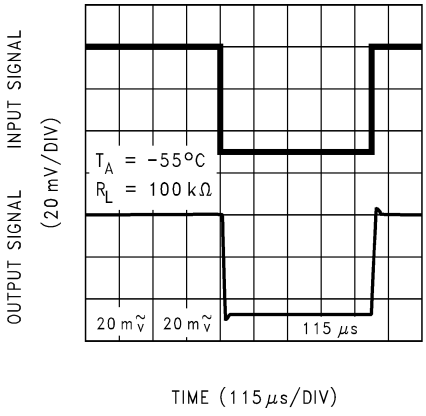

Figure 6-21. Noninverting Small-Signal Pulse Response

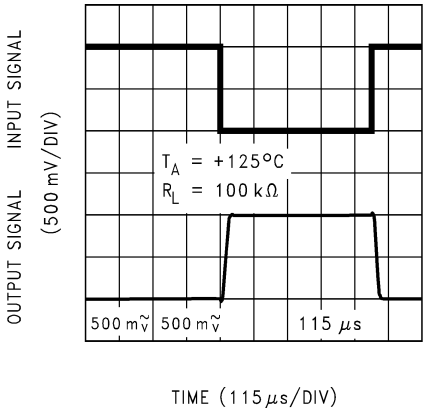

Figure 6-22. Inverting Large-Signal Pulse Response

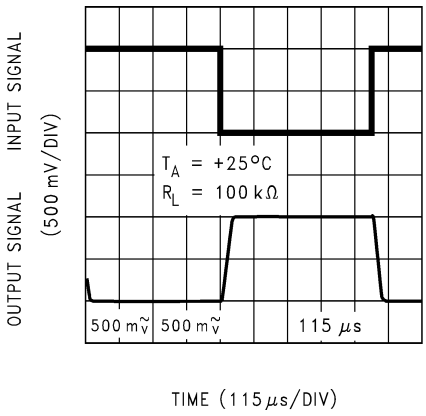

Figure 6-23. Inverting Large-Signal Pulse Response

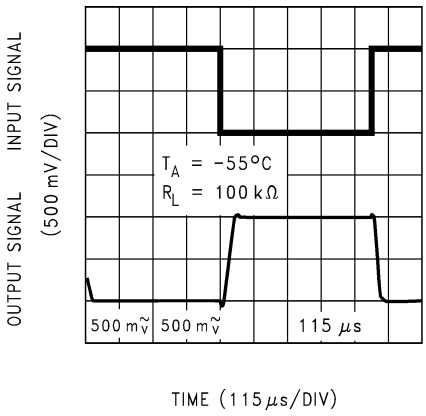

Figure 6-24. Inverting Large-Signal Pulse Response

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6 Typical Characteristics (continued)

at V_S = 5V, single supply, and T_A = 25°C (unless otherwise specified)

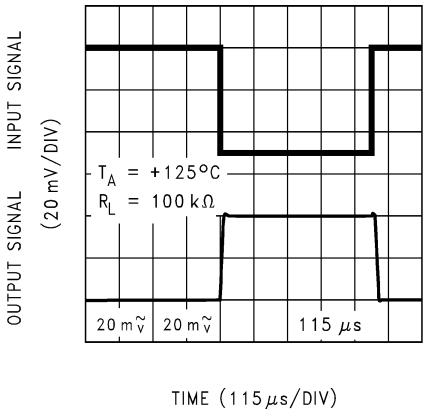

Figure 6-25. Inverting Small-Signal Pulse Response

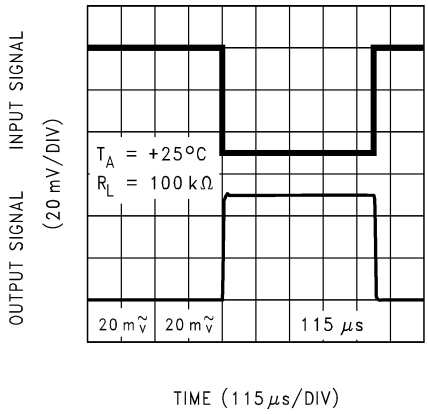

Figure 6-26. Inverting Small-Signal Pulse Response

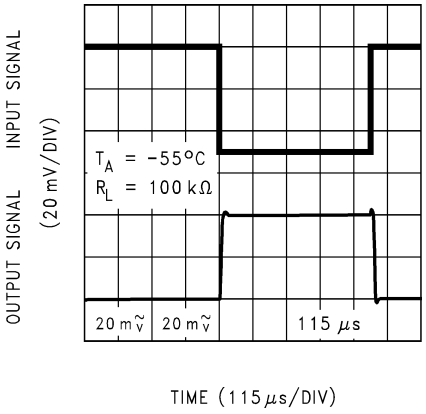

Figure 6-27. Inverting Small-Signal Pulse Response

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Input Common-Mode Voltage Range

The LMC646x have a rail-to-rail input common-mode voltage range. Some dc parameters such as input offset voltage, common-mode rejection, and power supply rejection can be degraded for common-mode voltages (V_{CM}) near the positive supply rail. The LMC646x is designed to achieve the best dc precision when the common-mode is limited to V_{CM} < (V+) − 2V. Figure 7-1 shows an input voltage exceeding both supplies with no resulting phase inversion on the output.

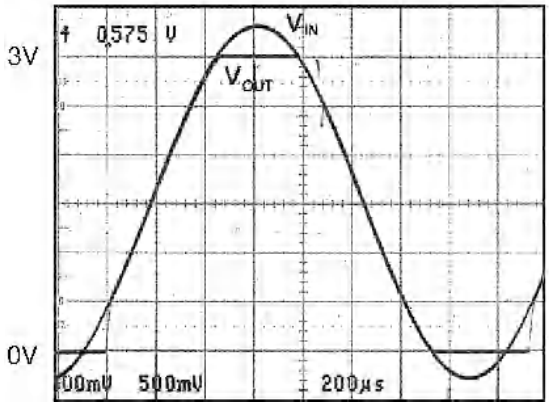

Figure 7-1. An Input Voltage Signal Exceeds the LMC646x Power Supply Voltage with No Output Phase Inversion

Figure 7-2. A ±7.5V Input Signal Greatly Exceeds the 3V Supply in Figure 7-3 Causing No Phase Inversion Due to R_I

The absolute maximum input voltage at V+ = 3V is 300mV beyond either supply rail at room temperature. Voltages greatly exceeding this absolute maximum rating, as in Figure 7-2, can cause excessive current to flow in or out of the input pins, possibly affecting reliability. The input current can be externally limited to ±5mA, with an input resistor, as shown in Figure 7-3.

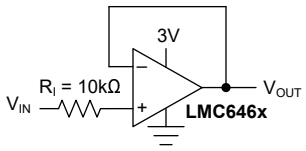

Figure 7-3. Input Current Protection for Voltages Exceeding the Supply Voltage

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7.1.2 Rail-to-Rail Output

The approximated output resistance of the LMC646x is 180Ω sourcing, and 130Ω sinking at V_S = 3V, and 110Ω sourcing and 83Ω sinking at V_S = 5V. The maximum output swing can be estimated as a function of load using the calculated output resistance.

7.1.3 Capacitive Load Tolerance

The LMC646x can typically drive a 200pF load with V_S = 5V at unity gain without oscillating. The unity gain follower is the most sensitive configuration to capacitive load. Direct capacitive loading reduces the phase margin of op amps. The combination of the op amp output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in Figure 7-4. If there is a resistive component of the load in parallel to the capacitive component, the isolation resistor and the resistive load create a voltage divider at the output. This introduces a DC error at the output.

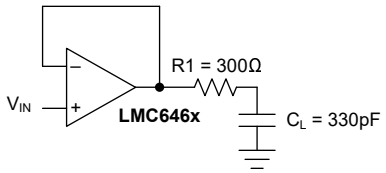

Figure 7-4. Resistive Isolation of a 300pF Capacitive Load

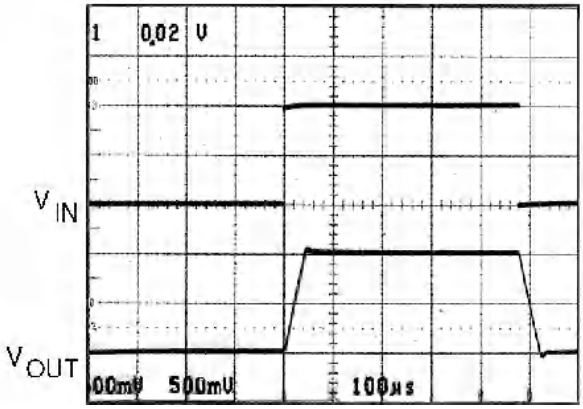

Figure 7-5. Pulse Response of the LMC6462 Circuit Shown in Figure 7-4

Figure 7-5 displays the pulse response of the LMC646x circuit in Figure 7-4.

Another circuit, shown in Figure 7-6, is also used to indirectly drive capacitive loads. This circuit is an improvement to the circuit shown in Figure 7-4 because Figure 7-6 provides dc accuracy as well as ac stability. R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifiers inverting input, thereby preserving phase margin in the overall feedback loop. The values of R1 and C1 can be experimentally determined by the system designer for the desired pulse response. Increased capacitive drive is possible by increasing the value of the capacitor in the feedback loop.

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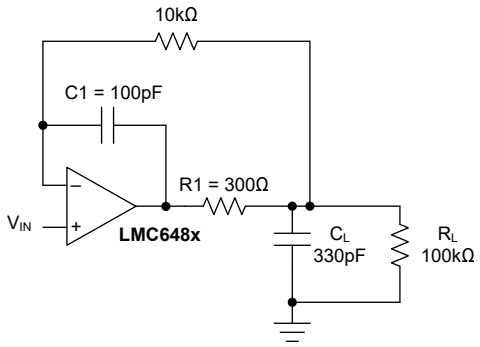

Figure 7-6. Noninverting Amplifier, Compensated to Handle a 300pF Capacitive and 100kΩ Resistive Load

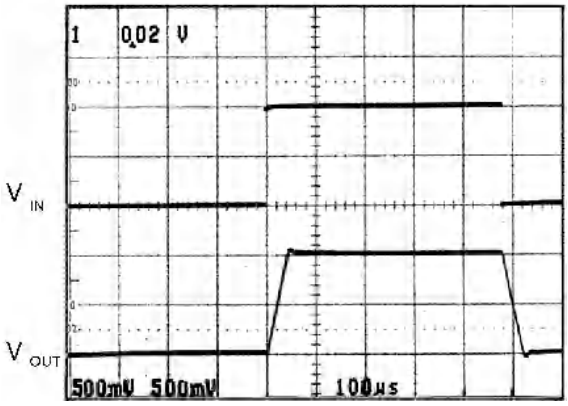

Figure 7-7. Pulse Response of LMC6462 Circuit in Figure 7-6

The pulse response of the circuit shown in Figure 7-6 is shown in Figure 7-7

7.1.4 Compensating for Input Capacitance

The use of large values of feedback resistance is quite common to do with amplifiers that have ultra-low input current, like the LMC646x. Large feedback resistors can react with small values of input capacitance due to transducers, photodiodes, and circuits board parasitics to reduce phase margins.

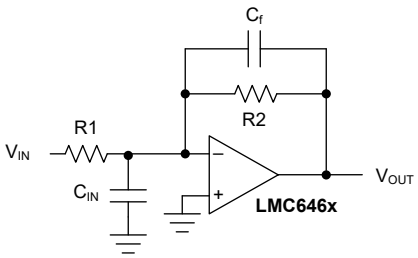

Figure 7-8. Canceling the Effect of Input Capacitance

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The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in Figure 7-8), C_F, is first estimated by:

$$\frac{1}{2\pi R1 C_{IN}} \geq \frac{1}{2\pi R2 C_F} \quad (1)$$

or

$$R1 C_{IN} \leq R2 C_F \quad (2)$$

which typically provides significant overcompensation.

Printed circuit board stray capacitance can be larger or smaller than that of a breadboard, so the actual optimum value for C_F can be different. Check the values of C_F on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

7.1.5 Offset Voltage Adjustment

Offset voltage adjustment circuits are illustrated in Figure 7-9 and Figure 7-10. Large-value resistances and potentiometers are used to reduce power consumption while providing typically ±2.5mV of adjustment range, referred to the input, for both configurations with V_S = ±5V.

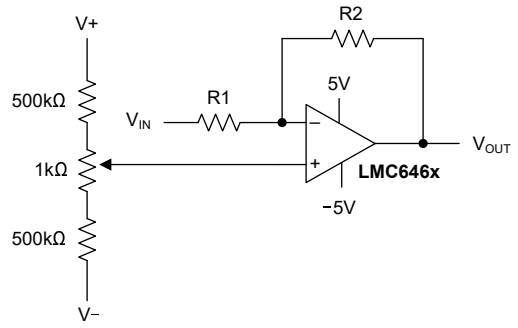

Figure 7-9. Inverting Configuration Offset Voltage Adjustment

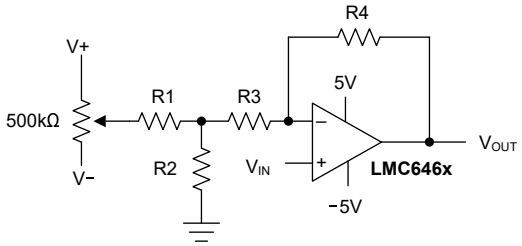

Figure 7-10. Noninverting Configuration Offset Voltage Adjustment

7.1.6 Instrumentation Circuits

The LMC646x has the high input impedance, large common-mode range and high CMRR needed for designing instrumentation circuits. Instrumentation circuits designed with the LMC646x can reject a larger range of common-mode signals than most in-amps. This makes instrumentation circuits designed with the LMC646x an excellent choice for noisy or industrial environments. Other applications that benefit from these features include analytic medical instruments, magnetic field detectors, gas detectors, and silicon-based transducers.

A small valued potentiometer is used in series with R_G to set the differential gain of the three op-amp instrumentation circuit in Figure 7-11. This combination is used instead of one large valued potentiometer to increase gain trim accuracy and reduce error due to vibration.

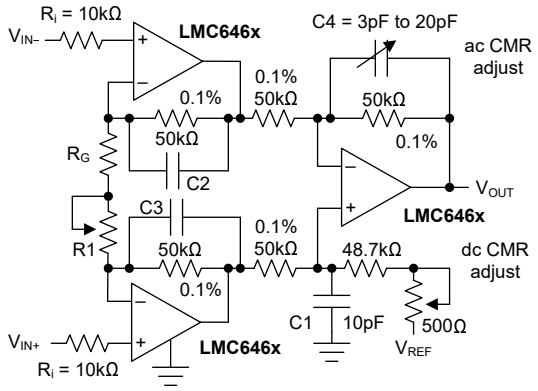

Figure 7-11. Low-Power Three Op-Amp Instrumentation Amplifier

A two op-amp instrumentation amplifier designed for a gain of 100 is shown in Figure 7-12. Low sensitivity trimming is made for offset voltage, CMRR and gain. Low cost and low power consumption are the main advantages of this two op-amp circuit.

Higher frequency and larger common-mode range applications are best facilitated by a three op-amp instrumentation amplifier.

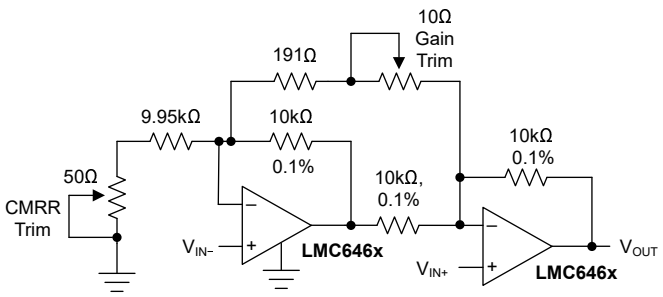

Figure 7-12. Low-Power Two Op Amp Instrumentation Amplifier

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7.2 Typical Applications

7.2.1 Transducer Interface Circuits

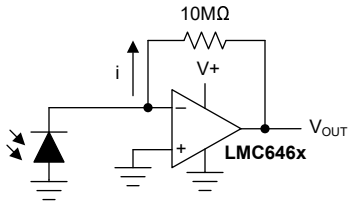

Figure 7-13. Photo Detector Circuit

Photocells can be used in portable light measuring instructions. The LMC646x, which can be operated off a battery, is an excellent choice for this circuit because of the very low input current and offset voltage performance.

7.2.2 LMC646x as a Comparator

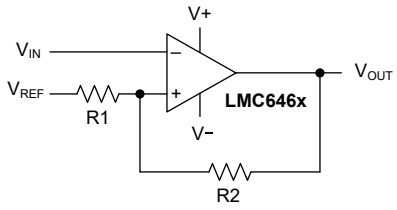

Figure 7-14. Comparator with Hysteresis

Figure 7-14 shows the application of the LMC646x as a comparator. The hysteresis is determined by the ratio of the two resistors. The LMC646x can thus be used as a micropower comparator, in applications where the quiescent current is an important parameter.

7.2.3 Half-Wave and Full-Wave Rectifiers

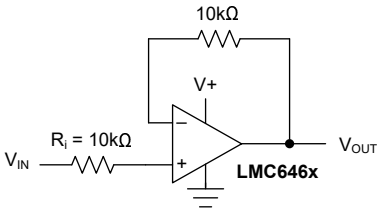

Figure 7-15. Half-Wave Rectifier with Input Current Protection (R_i)

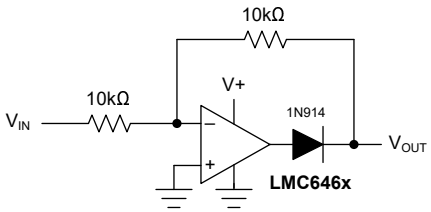

Figure 7-16. Full-Wave Rectifier with Input Current Protection (R_i)

In Figure 7-15 Figure 7-16, R_i limits current into the amplifier since excess current can be caused by the input voltage exceeding the supply voltage.

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7.2.4 Precision Current Source

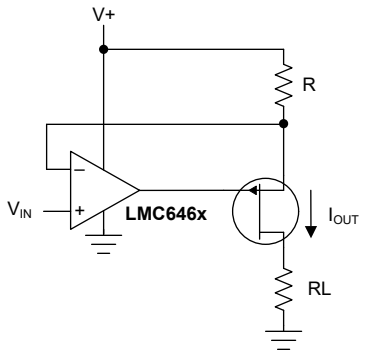

Figure 7-17. Precision Current Source

The output current I_{OUT} is given by:

$$I_{OUT} = \frac{(V+) - (V_{IN})}{R} \quad (3)$$

7.2.5 Oscillators

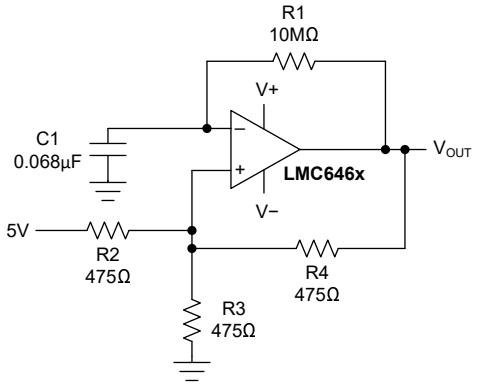

Figure 7-18. 1Hz Square-Wave Oscillator

For single supply 5V operation, the output of the circuit swings from 0V to 5V. The voltage divider set up by R_2, R_3 and R_4 cause the noninverting input of the LMC646x to move from 1.67V (1/3 of 5V) to 3.33V (2/3 of 5V). This voltage behaves as the threshold voltage.

R_1 and C_1 determine the time constant of the circuit. The frequency of oscillation, f_{OSC}, is:

$$\frac{1}{2\Delta t} \quad (4)$$

where

- Δt = time the amplifier input takes to move from 1.67V to 3.33V.

The calculations are as follows:

$$1.67 = 5\left(1 - e^{\frac{-t_1}{\tau}}\right) \quad (5)$$

where

- $\tau = RC = 0.68$ seconds
- $t_1 = 0.27$ seconds.

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and

$$3.33 = 5\left(1 - e^{\frac{-t_2}{\tau}}\right) \quad (6)$$

where

- t_2 = 0.75 seconds

Then,

$$f_{OSC} = \frac{1}{2\Delta t} = \frac{1}{2(0.75 - 0.27)} \cong 1\text{Hz} \quad (7)$$

7.2.6 Low Frequency Null

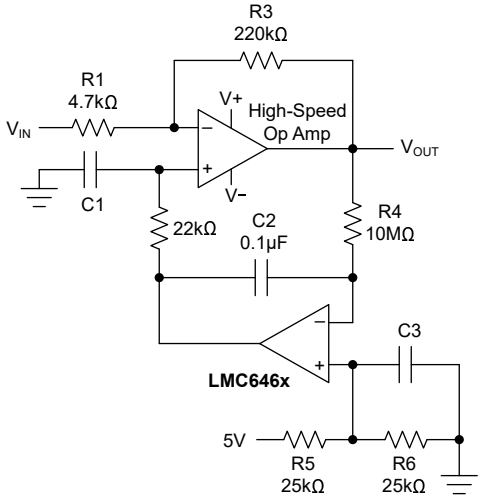

Figure 7-19. High Gain Amplifier with Low Frequency Null

Output offset voltage, V_{OS_OUT}, is the error introduced in the output voltage due to the inherent input offset voltage V_{OS}, of an amplifier.

$V_{OS_OUT} = V_{OS} \times$ Gain)

In the above configuration, the resistors R_5 and R_6 determine the nominal voltage around which the input signal, V_{IN}, is symmetrical. The high frequency component of V_{IN} is unaffected while the low frequency component is nulled since the dc level of the output is the input offset voltage of the LMC646x plus the bias voltage. This implies that the output offset voltage due to the top amplifier is eliminated.

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7.3 Layout

7.3.1 Layout Guidelines

7.3.1.1 PCB Layout for High-Impedance Work

As a general rule, any circuit that must operate with less than 1000pA of leakage current requires special layout of the printed circuit board (PCB). When one wishes to take advantage of the ultra-low input current of the LMC646x, typically 150fA, an excellent layout is essential. Fortunately, the techniques of obtaining low leakages are quite simple. First, do not ignore the surface leakage of the PCB, even though the leakage current can sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage can be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC646x inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, and so forth connected to the inputs of the op amp, as in Figure 7-20. To have a significant effect, place guard rings on both the top and bottom of the PCB. This PC foil must then be connected to a voltage that is at the same voltage as the amplifier inputs, because no leakage current can flow between two points at the same potential. For example, a PCB trace-to-pad resistance of 10^{12}, which is normally considered a very large resistance, can leak 5pA if the trace were a 5V bus adjacent to the pad of the input. This leakage can cause a 250 times degradation from the actual performance of the LMC646x. However, if a guard ring is held within 5mV of the inputs, then even a resistance of $10^{11}\Omega$ causes only 0.05pA of leakage current. See Figure 7-21 through Figure 7-23 for typical connections of guard rings for standard op-amp configurations

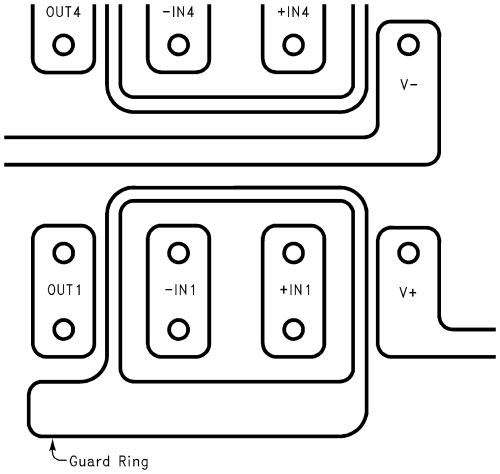

Figure 7-20. Example of Guard Ring in P.C. Board Layout

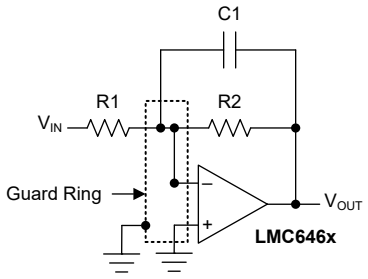

Figure 7-21. Typical Connections of Guard Rings – Inverting Amplifier

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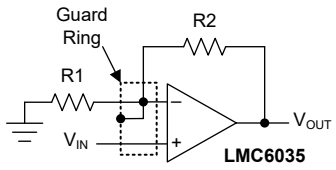


Figure 7-22. Typical Connections of Guard Rings – Non-Inverting Amplifier

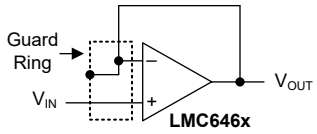
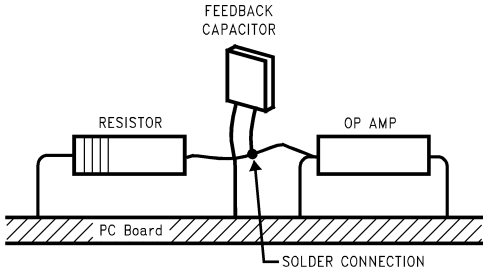


Figure 7-23. Typical Connections of Guard Rings – Follower

Be aware that when laying out a PCB for the sake of just a few circuits is not practical, another technique is even better than a guard ring on a PCB: Do not insert the input pin of the amplifier into the PCB at all, but bend the pin up in the air, and use only air as an insulator. Air is an excellent insulator. In this case you forgo some of the advantages of PCB construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 7-24.



(Input pins are lifted out of PCB and soldered directly to components. All other pins connected to PCB.)

Figure 7-24. Air Wiring

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Device Support

8.1.1 Development Support

8.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

8.2 Documentation Support

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
PSpice® is a registered trademark of Cadence Design Systems, Inc.
All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2013) to Revision E (March 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated first page figure	1
• Added *Pin Configuration and Functions*	2
• Deleted note 2 from *Absolute Maximum Ratings*	4
• Added *ESD Ratings*	4
• Added *Thermal Information*	5
• Updated parameter names and symbols in both *Electrical Characteristics*	6
• Deleted notes 1, 2, and 3 from previous DC *Electrical Characteristics*	6
• Deleted notes 1 and 2 from previous AC *Electrical Characteristics*	6

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- Moved note 4 conditions from previous DC *Electrical Characteristics* to open-loop gain test conditions..... 6
- Updated note 3 in previous AC *Electrical Characteristics* and moved conditions to slew rate test conditions...6
- Deleted phase margin from *Electrical Characteristics* 6
- Moved note 3 conditions from previous AC *Electrical Characteristics* to crosstalk test conditions..... 6
- Changed short-circuit current (V+ = 15V, sinking) TYP from 75mA to 38mA and MIN from 55mA to 28mA..... 6
- Changed short-circuit current (V+ = 15V, sinking, TJ = –40°C to +85°C) MIN from 45mA to 22mA.....6
- Added Figure 6-9 and Figure 6-10.....11
- Deleted Figures 12 to 15..... 11
- Updated description in *Input Common-Mode Voltage Range* 16

Changes from Revision C (March 2013) to Revision D (March 2013) **Page**

- Changed layout of National Data Sheet to TI format.....23

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMC6462AIM/NOPB	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	LMC64 62AIM
LMC6462AIMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC64 62AIM
LMC6462AIMX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC64 62AIM
LMC6462AIMX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC64 62AIM
LMC6462AIN/NOPB	Obsolete	Production	PDIP (P) | 8	-	-	Call TI	Call TI	-40 to 85	LMC6462 AIN
LMC6462BIM/NOPB	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	LMC64 62BIM
LMC6462BIMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC64 62BIM
LMC6462BIMX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC64 62BIM
LMC6462BIMX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC64 62BIM
LMC6462BIN/NOPB	Obsolete	Production	PDIP (P) | 8	-	-	Call TI	Call TI	-40 to 85	LMC6462 BIN
LMC6464AIM/NOPB	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	LMC6464 AIM
LMC6464AIMX/NOPB	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC6464 AIM
LMC6464AIMX/NOPB.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC6464 AIM
LMC6464AIMX/NOPB.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
LMC6464BIM/NOPB	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	LMC6464 BIM
LMC6464BIMX/NOPB	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC6464 BIM
LMC6464BIMX/NOPB.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMC6464 BIM

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMC6464BIMX/NOPB.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
LMC6464BIN/NOPB	Obsolete	Production	PDIP (N) | 14	-	-	Call TI	Call TI	-40 to 85	LMC6464BIN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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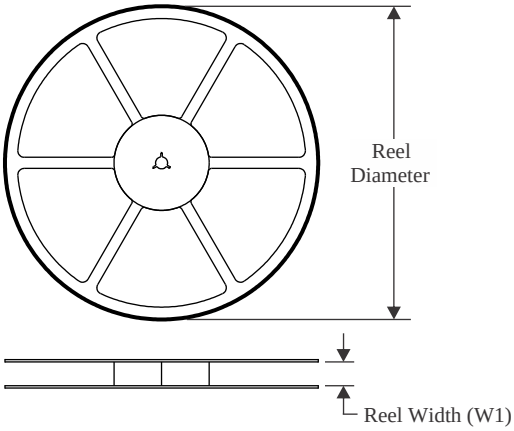
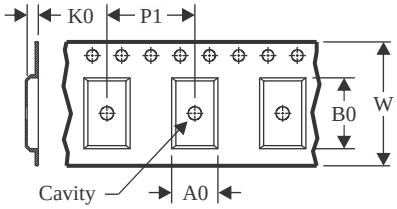
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

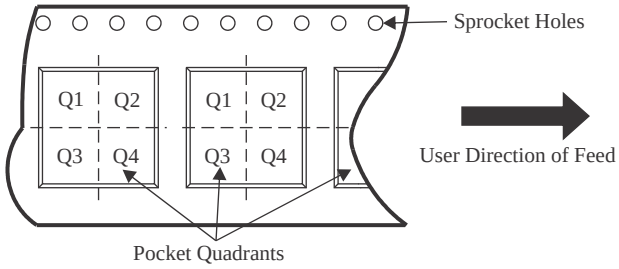


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

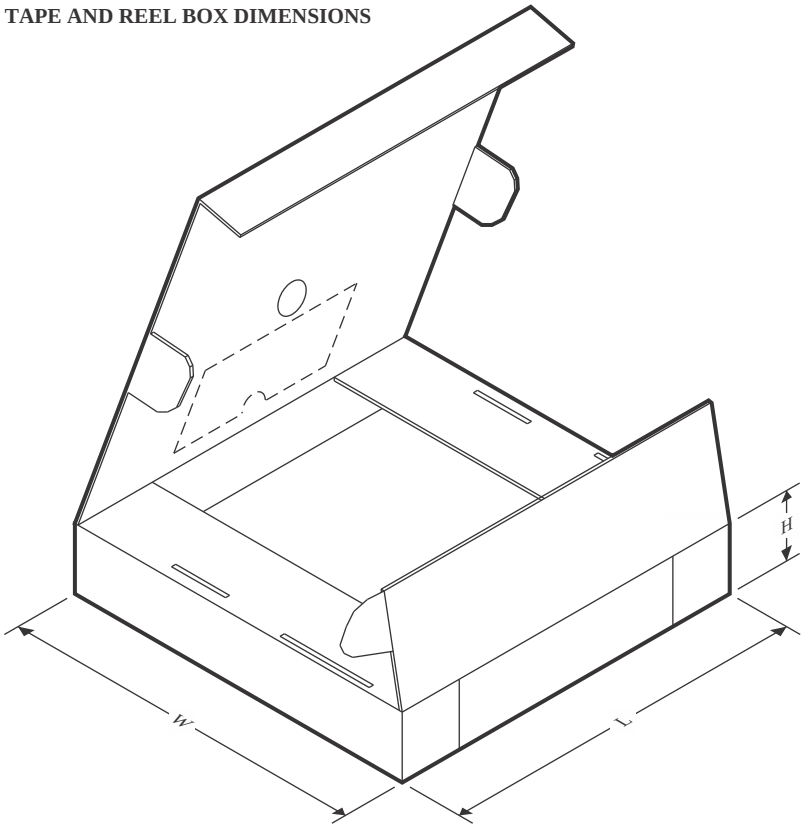
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

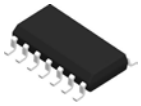
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC6462AIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6462BIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6464AIMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMC6464BIMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC6462AIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC6462BIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC6464AIMX/NOPB	SOIC	D	14	2500	356.0	356.0	35.0
LMC6464BIMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

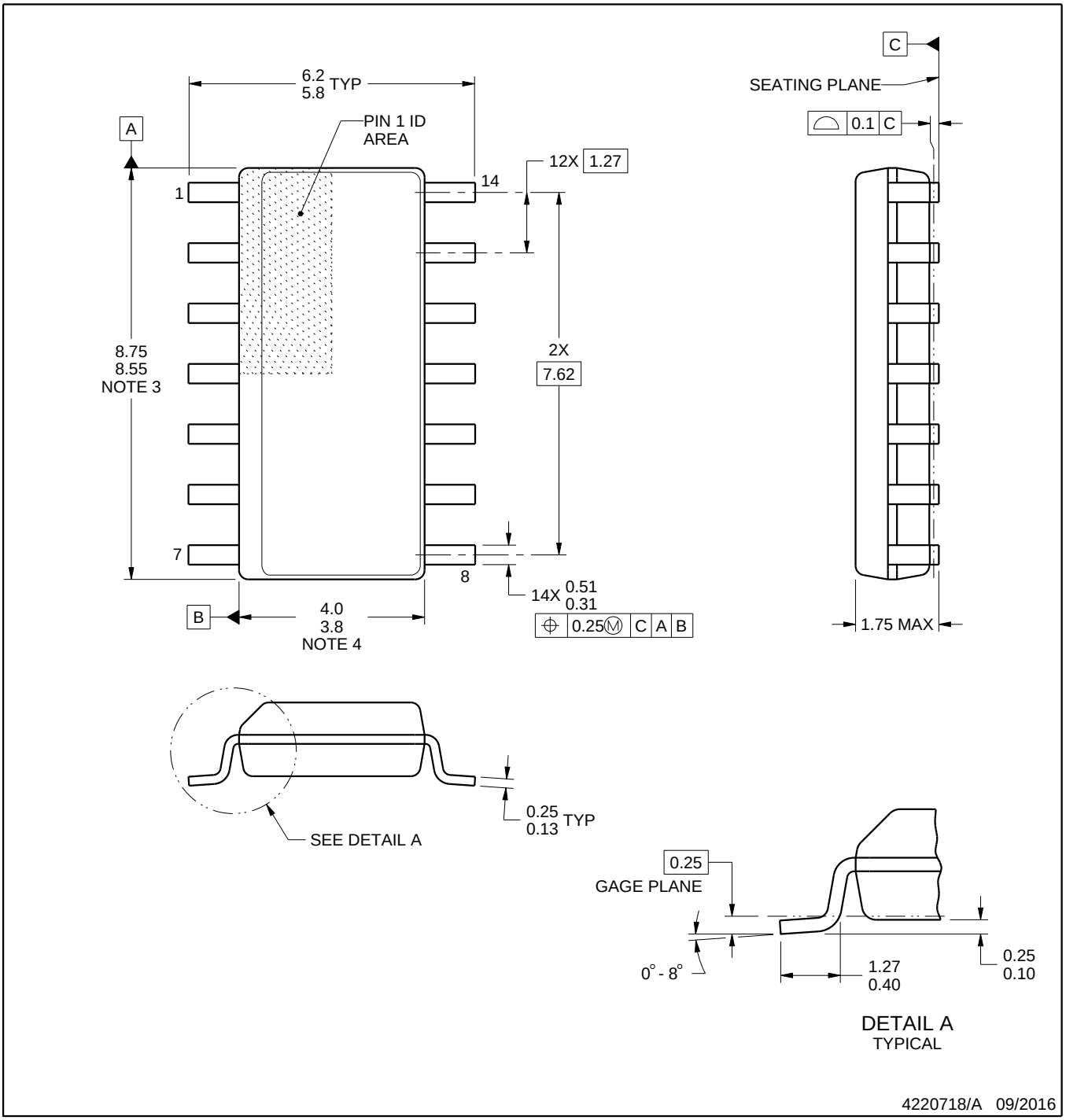


PACKAGE OUTLINE

D0014A

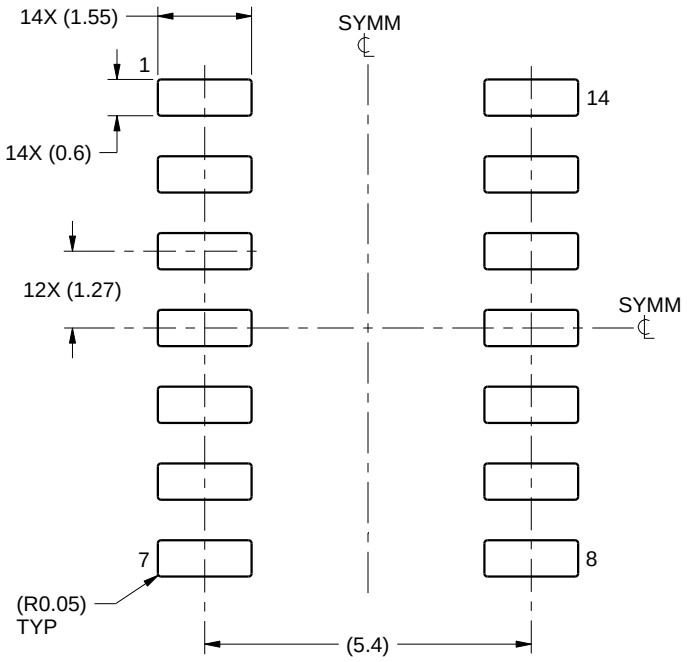
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

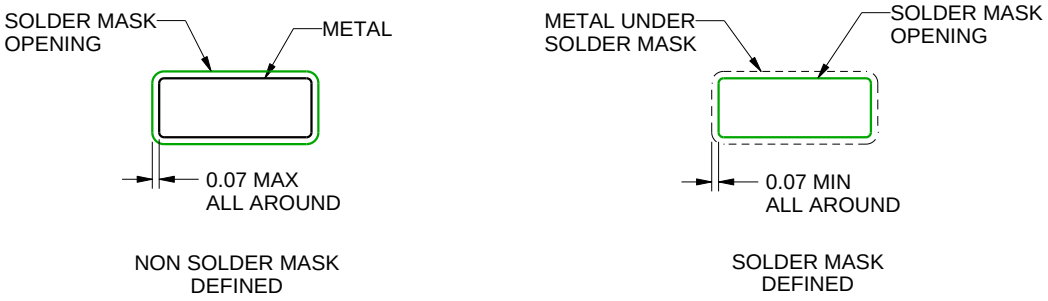


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

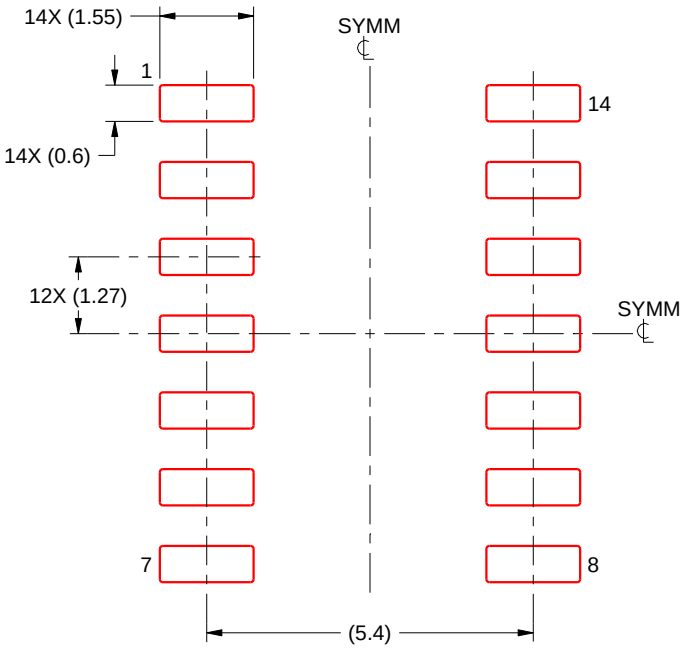
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

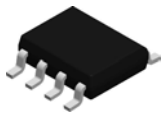


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

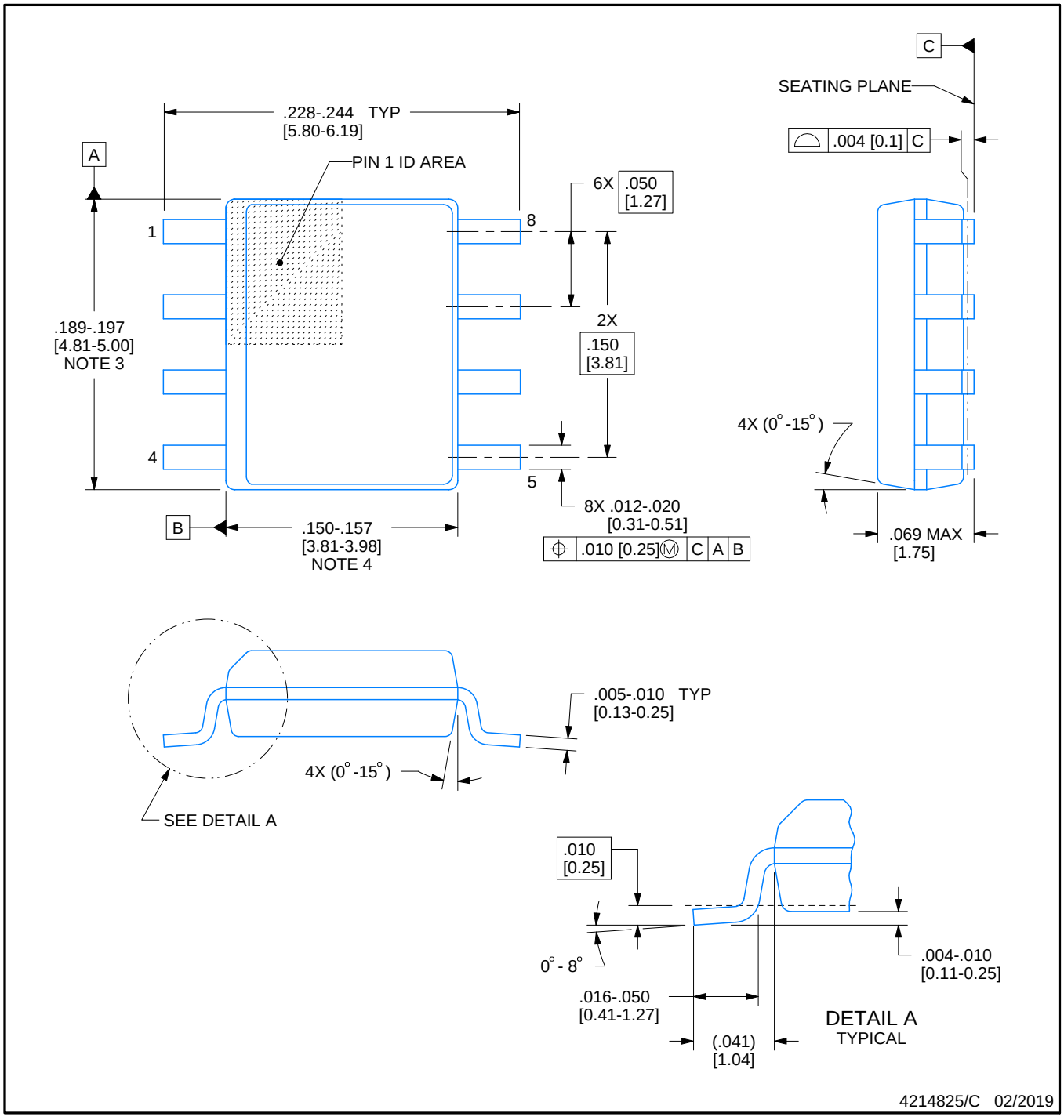


PACKAGE OUTLINE

D0008A

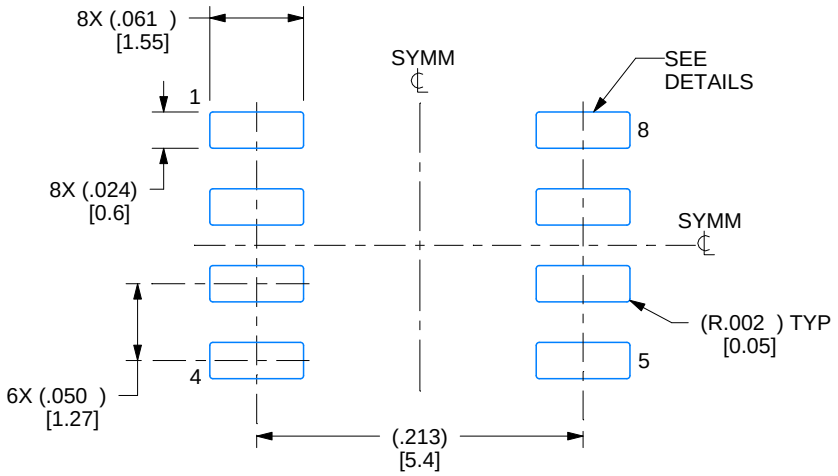
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

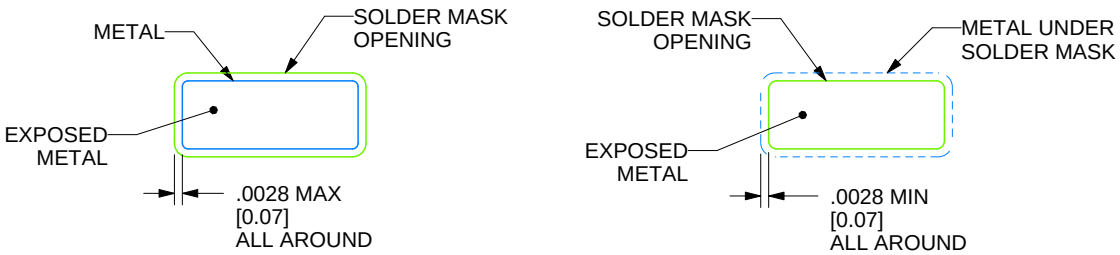


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

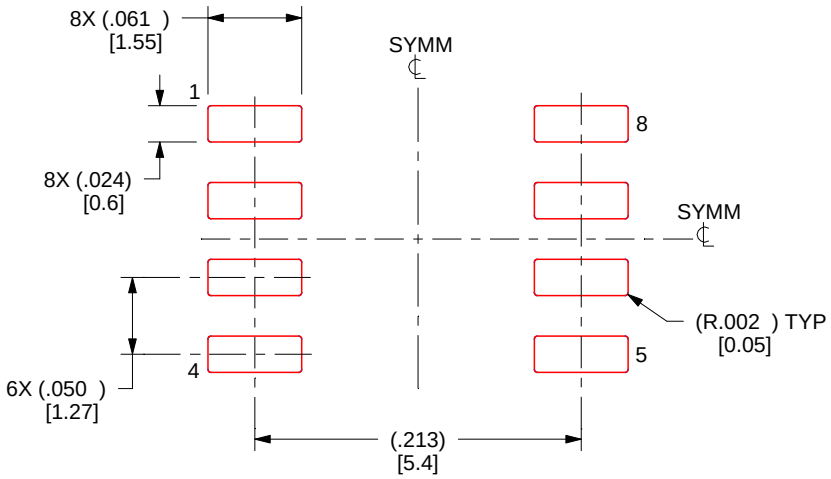
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



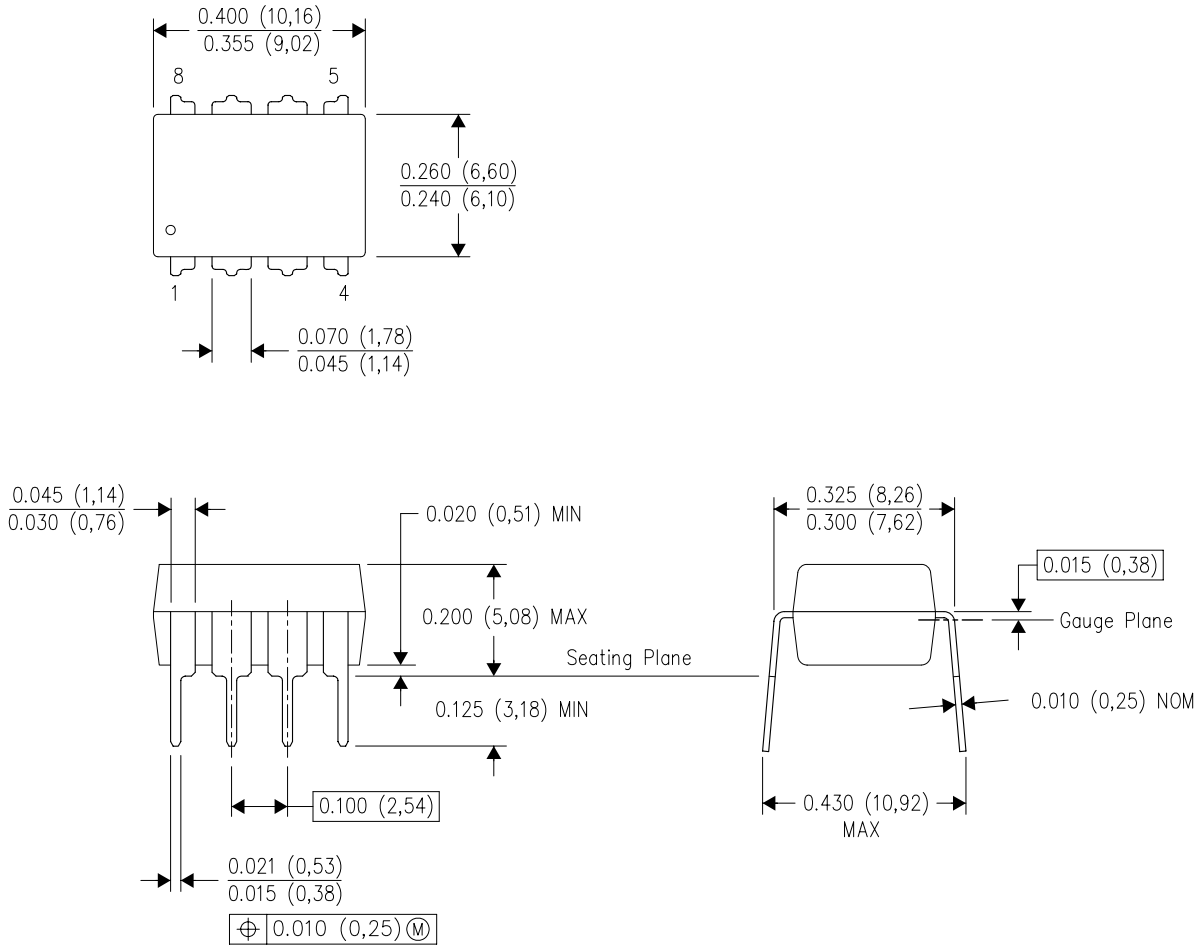
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

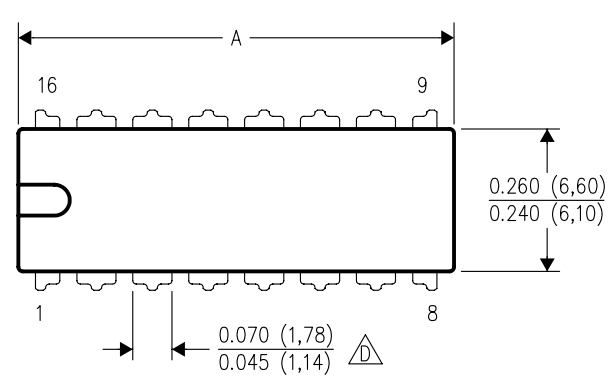


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

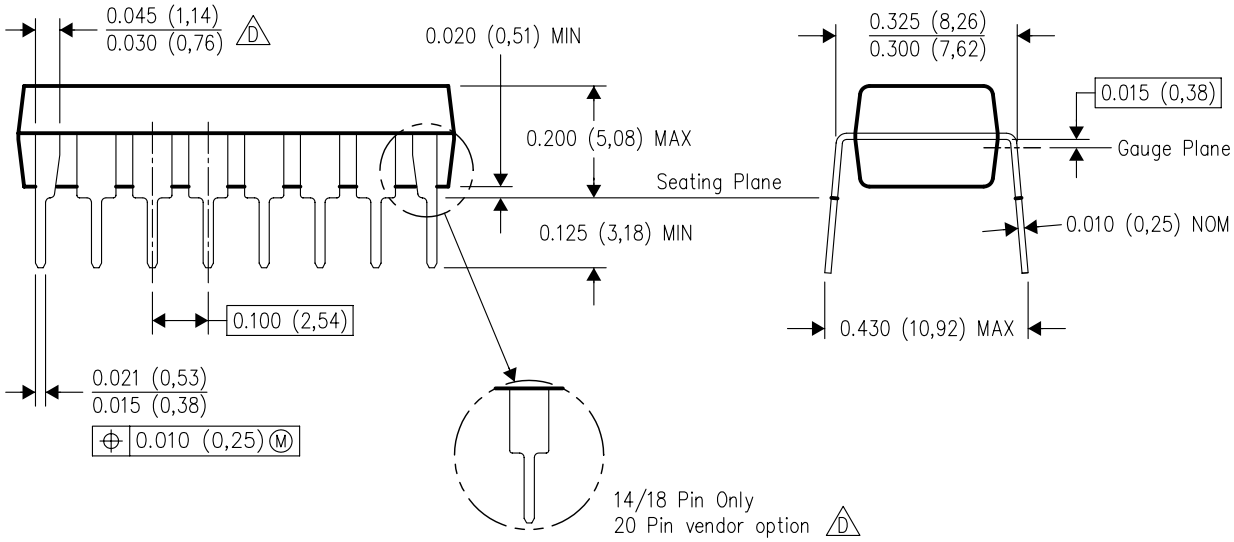
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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