

FEATURES

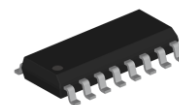
- Wide Operating Voltage Range of 2.0V to 6.0V
- 8-Bit Serial-Input, Serial or Parallel-Out Shift
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices

APPLICATIONS

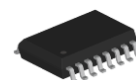
- Network Switches
- Power Infrastructure
- LED Displays
- Servers

DESCRIPTION

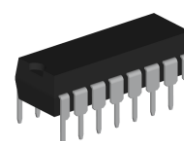
The 74HC595 devices contain an 8-bit, serial-in, parallel-out shift register that feeds an 8-bit D-type latch with parallel 3-state outputs. Separate clocks are provided for both the shift register and latch. The shift register has a direct overriding clear input, serial input, and serial outputs for cascading. This device also has an asynchronous reset for the shift register.



SOP-16



TSSOP-16



DIP-16

ORDERING INFORMATION

Device	Package
74HC595D	SOP-16
74HC595TD	TSSOP-16
74HC595N	DIP-16

ABSOLUTE MAXIMUM RATINGS (Note 1)

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5	7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-0.5	$V_{CC} + 0.5$	V
DC Output Voltage (Referenced to GND)	V_{OUT}	-0.5	$V_{CC} + 0.5$	V
DC Input Current	I_{IN}	-	± 20	mA
DC Output Current	I_{OUT}	-	± 35	mA
DC Supply Current	I_{CC}	-	± 75	mA
Maximum Junction Temperature	T_J	-	150	$^{\circ}$ C
Storage Temperature	T_{STG}	-65	150	$^{\circ}$ C

Note1. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8-Bit Shift Registers With Latched 3-State Outputs

74HC595

RECOMMENDED OPERATING CONDITIONS (Note 2)

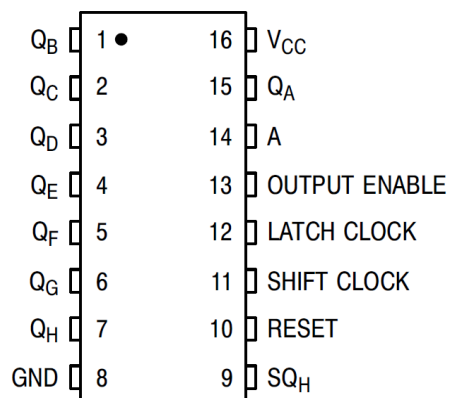
CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
Supply Voltage	V_{CC}	2.0	6.0	V
DC Input Voltage	V_{IN}	0	V_{CC}	V
DC Output Voltage	V_{OUT}	0	V_{CC}	V
Operating Free-Air Temperature Range	T_A	-55	125	°C

Note 2. The device is not guaranteed to function outside its operating ratings.

ORDERING INFORMATION

Package	Order No.	Description	Package Marking	Status
SOP-16	74HC595D	8-Bit Shift Registers	74HC595	Active
TSSOP-16	74HC595TD	8-Bit Shift Registers	74HC595	Active
DIP-16	74HC595N	8-Bit Shift Registers	74HC595	Active

PIN CONFIGURATION

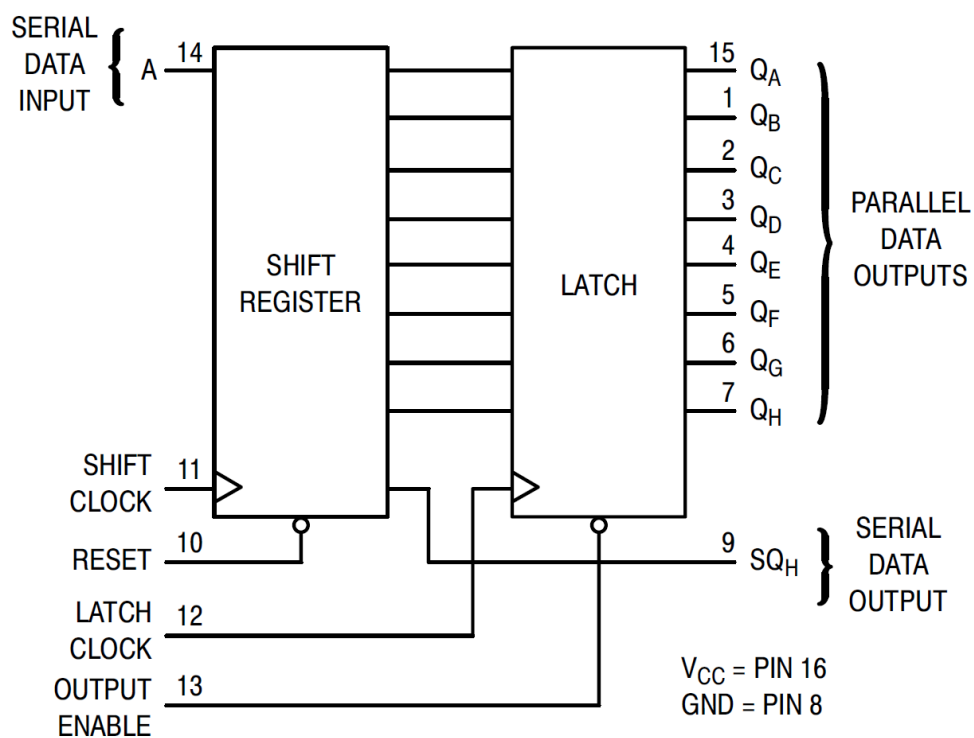


SOP-16 / TSSOP-16 / DIP-16

PIN DESCRIPTION

Pin No.			Pin Name	Pin Function
SOP-16	TSSOP-16	DIP-16		
1	1	1	QB	Parallel Data QB Output
2	2	2	QC	Parallel Data QC Output
3	3	3	QD	Parallel Data QD Output
4	4	4	QE	Parallel Data QE Output
5	5	5	QF	Parallel Data QF Output
6	6	6	QG	Parallel Data QG Output
7	7	7	QH	Parallel Data QH Output
8	8	8	GND	Ground
9	9	9	SQH	Serial Data Output
10	10	10	RESET	Shift Register Reset Input
11	11	11	SHIFT CLOCK	Shift Register Clock Input.
12	12	12	LATCH CLOCK	Parallel Latch Clock Input
13	13	13	OUTPUT ENABLE	Output Enable
14	14	14	A	Serial Data Input
15	15	15	QA	Parallel Data QA Output
16	16	16	VCC	Power Supply

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

Voltages referenced to ground.

SYMBOL	PARAMETER	TEST CONDITION	VCC	Limit			UNIT
				≤ 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ $ I_{OUT} \leq 20 \mu A$	2.0 V	1.50	1.50	1.50	V
			4.5 V	3.15	3.15	3.15	
			6.0 V	4.20	4.20	4.20	
V_{IL}	Maximum Low-Level Input Voltage	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ $ I_{OUT} \leq 20 \mu A$	2.0 V	0.50	0.50	0.50	V
			4.5 V	1.35	1.35	1.35	
			6.0 V	1.80	1.80	1.80	
V_{OH}	Minimum High-Level Output Voltage, $Q_A - Q_H$	$V_{IN} = V_{IH}$ or V_{IL}	$ I_{OUT} \leq 20 \mu A$	2.0 V	1.9	1.9	V
				4.5 V	4.4	4.4	
				6.0 V	5.9	5.9	
			$ I_{OUT} \leq 6.0 \text{ mA}$	4.5 V	3.98	3.84	
				6.0 V	5.48	5.34	
V_{OL}	Maximum Low-Level Output Voltage, $Q_A - Q_H$	$V_{IN} = V_{IH}$ or V_{IL}	$ I_{OUT} \leq 20 \mu A$	2.0 V	0.1	0.1	V
				4.5 V	0.1	0.1	
				6.0 V	0.1	0.1	
			$ I_{OUT} \leq 6.0 \text{ mA}$	4.5 V	0.26	0.33	
				6.0 V	0.26	0.33	
V_{OH}	Minimum High-Level Output Voltage, SQ_H	$V_{IN} = V_{IH}$ or V_{IL}	$ I_{OUT} \leq 20 \mu A$	2.0 V	1.9	1.9	V
				4.5 V	4.4	4.4	
				6.0 V	5.9	5.9	
			$ I_{OUT} \leq 4.0 \text{ mA}$	4.5 V	3.98	3.84	
				6.0 V	5.48	5.34	
V_{OL}	Maximum Low-Level Output Voltage, SQ_H	$V_{IN} = V_{IH}$ or V_{IL}	$ I_{OUT} \leq 20 \mu A$	2.0 V	0.1	0.1	V
				4.5 V	0.1	0.1	
				6.0 V	0.1	0.1	
			$ I_{OUT} \leq 4.0 \text{ mA}$	4.5 V	0.26	0.33	
				6.0 V	0.26	0.33	
I_{IN}	Maximum Input Leakage Current	$V_{IN} = V_{CC}$ or GND	6.0 V	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current, $Q_A - Q_H$	Output in High-Impedance State $V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	6.0 V	±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	6.0 V	4.0	40	160	μA

AC ELECTRICAL CHARACTERISTICS

C_L = 50 pF, Input t_r = t_f = 6.0 ns

SYMBOL	PARAMETER	VCC	Limit			UNIT
			≤ 25°C	≤ 85°C	≤ 125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 7)	2.0 V	6.0	4.8	4.0	MHz
		4.5 V	30	24	20	
		6.0 V	35	28	24	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Shift Clock to SQ _H (Figures 1 and 7)	2.0 V	140	175	210	ns
		4.5 V	28	35	42	
		6.0 V	24	30	36	
t _{PHL}	Maximum Propagation Delay, Reset to SQ _H (Figures 2 and 7)	2.0 V	145	180	220	ns
		4.5 V	29	36	44	
		6.0 V	25	31	38	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Latch Clock to Q _A – Q _H (Figures 3 and 7)	2.0 V	140	175	210	ns
		4.5 V	28	35	42	
		6.0 V	24	30	36	
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Q _A – Q _H (Figures 4 and 8)	2.0 V	150	190	225	ns
		4.5 V	30	38	45	
		6.0 V	26	33	38	
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Q _A – Q _H (Figures 4 and 8)	2.0 V	135	170	205	ns
		4.5 V	27	34	41	
		6.0 V	23	29	35	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Q _A – Q _H (Figures 3 and 7)	2.0 V	60	75	90	ns
		4.5 V	12	15	18	
		6.0 V	10	13	15	
t _{TLH} , t _{THL}	Maximum Output Transition Time, SQ _H (Figures 1 and 7)	2.0 V	75	95	110	ns
		4.5 V	15	19	22	
		6.0 V	13	16	19	
C _{IN}	Maximum Input Capacitance	–	10	10	10	pF
C _{OUT}	Maximum Three-State Output Capacitance (Output in High-Impedance State), Q _A – Q _H	–	15	15	15	pF
C _{PD}	Power Dissipation Capacitance (per Package) (Note 3)	5.0 V	300 @ 25°C			pF

Note 3. Used to determine the no-load dynamic power consumption: P_D = C_{PD}V_{CC}²f + I_{CC}V_{CC}.

TIMING REQUIREMENTS

C_L = 50 pF, Input t_r = t_f = 6.0 ns

SYMBOL	PARAMETER	VCC	Limit			UNIT
			≤ 25°C	≤ 85°C	≤ 125°C	
t _{su}	Minimum Setup Time, Serial Data Input A to Shift Clock (Figure 5)	2.0 V	50	65	75	MHz
		4.5 V	10	13	15	
		6.0 V	9	11	13	
t _{su}	Minimum Setup Time, Shift Clock to Latch Clock (Figure 6)	2.0 V	75	95	110	ns
		4.5 V	15	19	22	
		6.0 V	13	16	19	
t _h	Minimum Hold Time, Shift Clock to Serial Data Input A (Figure 5)	2.0 V	5	5	5	ns
		4.5 V	5	5	5	
		6.0 V	5	5	5	
t _{rec}	Minimum Recovery Time, Reset Inactive to Shift Clock (Figure 2)	2.0 V	50	65	75	ns
		4.5 V	10	13	15	
		6.0 V	9	11	13	
t _w	Minimum Pulse Width, Reset (Figure 2)	2.0 V	60	75	90	ns
		4.5 V	12	15	18	
		6.0 V	10	13	15	
t _w	Minimum Pulse Width, Shift Clock (Figure 1)	2.0 V	50	65	75	ns
		4.5 V	10	13	15	
		6.0 V	9	11	13	
t _w	Minimum Pulse Width, Latch Clock (Figure 6)	2.0 V	50	65	75	ns
		4.5 V	10	13	15	
		6.0 V	9	11	13	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0 V	1000	1000	1000	ns
		4.5 V	500	500	500	
		6.0 V	400	400	400	

FUNCTION TABLE

Operation	Inputs					Resulting Function			
	Reset	Serial Input A	Shift Clock	Latch Clock	Output Enable	Shift Register Contents	Latch Register Contents	Serial Output SQ _H	Parallel Outputs Q _A – Q _H
Reset shift register	L	X	X	L, H, ↓	L	L	U	L	U
Shift data into shift register	H	D	↑	L, H, ↓	L	D→SR _A ; SR _N →SR _{N+1}	U	SR _G →SR _H	U
Shift register remains unchanged	H	X	L, H, ↓	L, H, ↓	L	U	U	U	U
Transfer shift register contents to latch register	H	X	L, H, ↓	↑	L	U	SR _N →LR _N	U	SR _N
Latch register remains unchanged	X	X	X	L, H, ↓	L	*	U	*	U
Enable parallel outputs	X	X	X	X	L	*	**	*	Enabled
Force outputs into high impedance state	X	X	X	X	H	*	**	*	Z

SR: shift register contents

LR: latch register contents

X: don't care

Z: high impedance

D: data (L, H) logic level

U: remains unchanged

*: depends on Reset and Shift Clock inputs

**: depends on Latch Clock input

↑: Low-to-High

↓: High-to-Low

SWITCHING WAVEFORMS

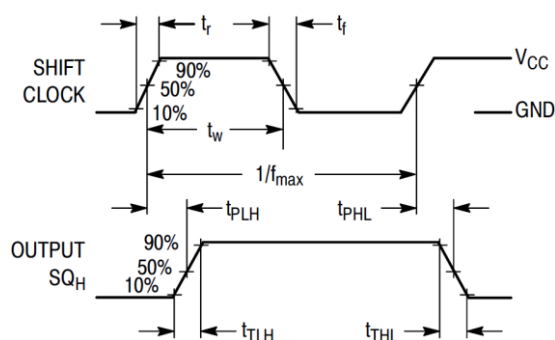


Fig. 1.

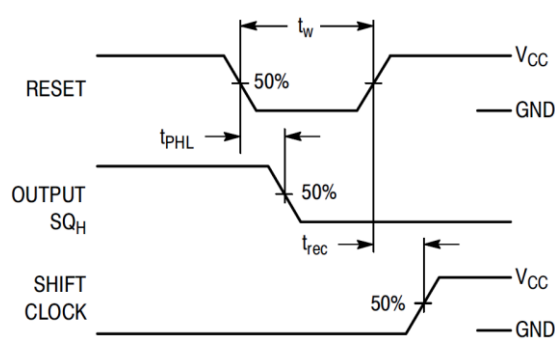


Fig. 2.

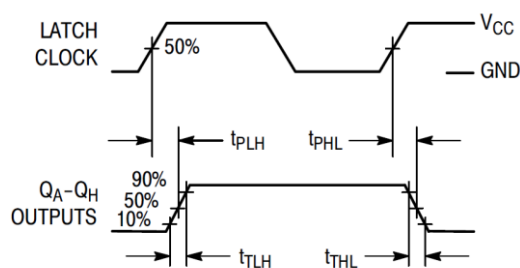


Fig. 3.

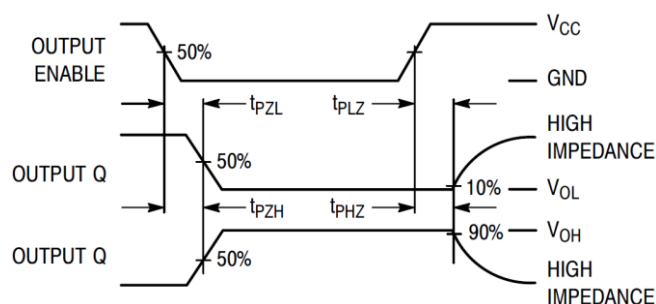


Fig. 4.

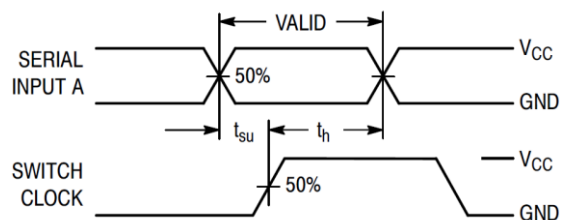


Fig. 5.

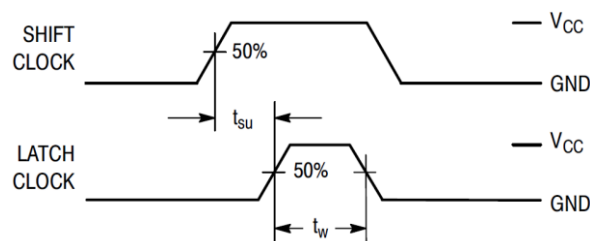
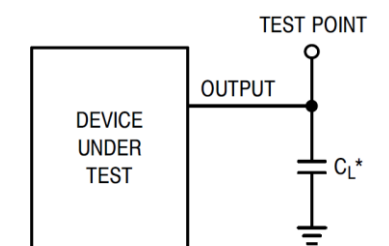


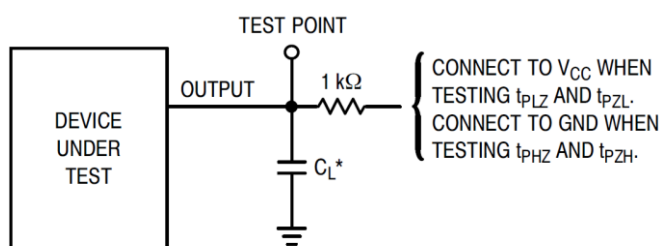
Fig. 6.

TEST CIRCUITS



*Includes all probe and jig capacitance

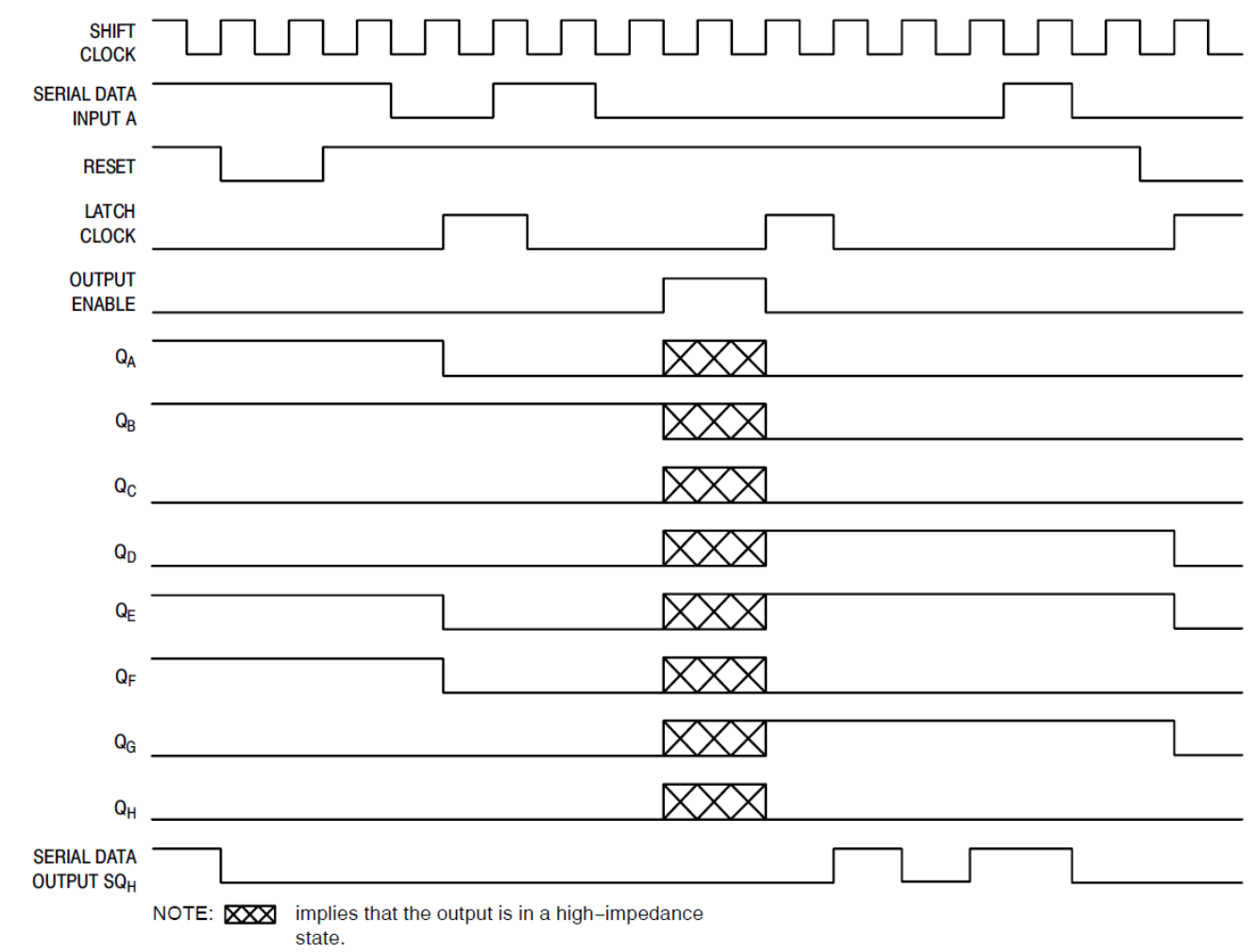
Fig. 7.



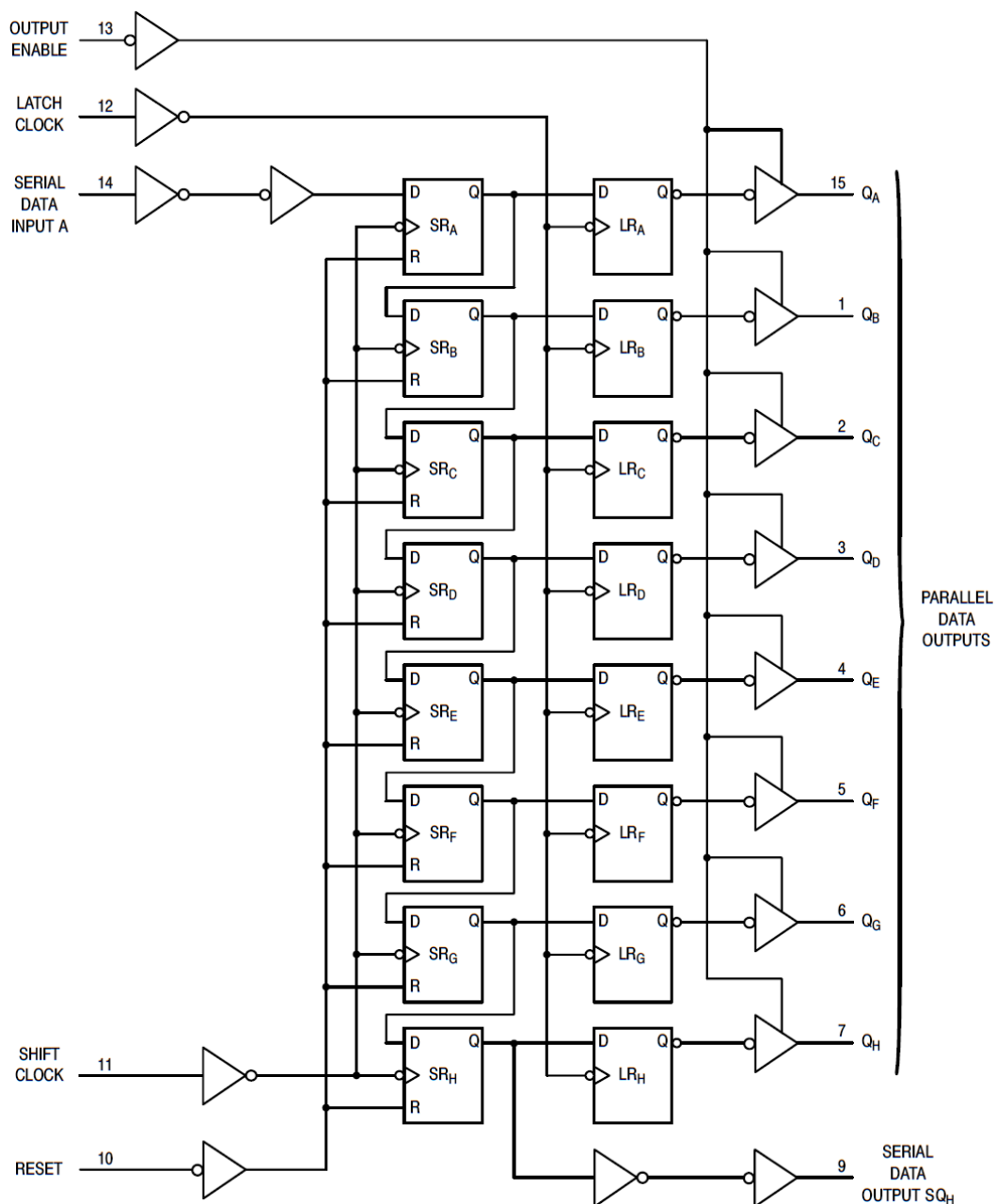
*Includes all probe and jig capacitance

Fig. 8.

TIMING DIAGRAM



FUNCTIONAL LOGIC DIAGRAM



TYPICAL OPERATING CHARACTERISTICS

T.B.D.

REVISION NOTICE

The description in this datasheet is subject to change without any notice to describe its electrical characteristics properly.