SNx4AHCT373 Octal Transparent D-Type Latches With 3-State Outputs

1 Features

- Operating range 4.5V to 5.5V V_{CC}
- TTL-Compatible inputs
- Low delay, 9.5ns (5V V_{CC} at C_L = 15pF)
- Latch-up performance exceeds 250mA per JESD 17
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

2 Applications

- Parallel data storage
- Digital bus buffer

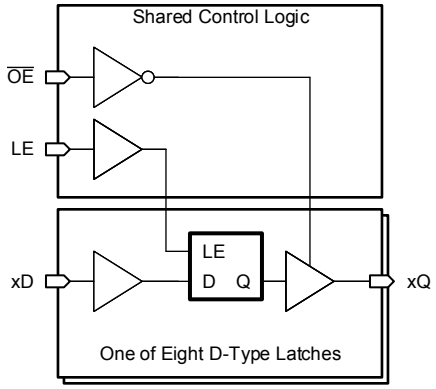
3 Description

The SNx4AHCT373 contains eight D-type latches. All channels share a latch enable (LE) input and output enable ($\overline{OE}$) input.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
SN54AHCT373	J (CDIP, 20)	24.2mm x 7.62mm	24.2mm x 6.92mm
	W (CFP, 20)	13.09mm x 8.13mm	13.09mm x 6.92mm
	FK (LCCC, 20)	8.89mm × 8.89mm	8.89mm × 8.89mm
SN74AHCT373	PW (TSSOP, 20)	6.5mm × 6.4mm	6.5mm x 4.4mm
	DW (SOIC, 20)	12.80mm × 10.3mm	12.8mm x 7.5mm
	DB (SSOP, 20)	7.2mm × 7.8mm	7.50mm x 5.3mm
	NS (SOP, 20)	12.6mm x 7.8mm	12.6mm x 5.3mm
	N (PDIP, 20)	24.33mm x 9.4mm	25.4mm x 6.35mm
	DGS (VSSOP, 20)	5.1mm × 4.9mm	5.1mm × 3.0mm
	RKS (VQFN, 20)	4.5mm × 2.5mm	4.5mm × 2.5mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Functional Block Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

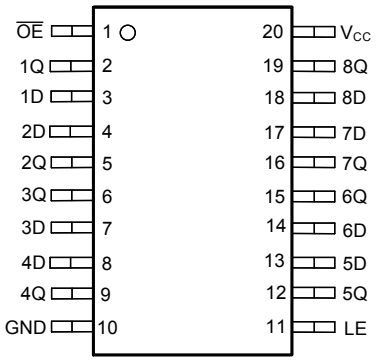


Figure 4-1. SN54AHCT373 J , W Package (Top View)

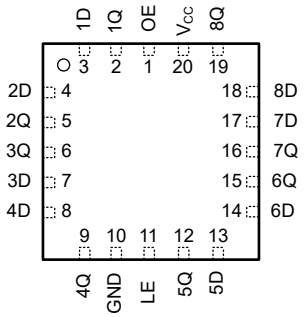


Figure 4-2. SN54AHCT373 FK Package (Top View)

Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
$\overline{OE}$	1	I	Output enable, active low
1Q	2	O	Output for channel 1
1D	3	I	Input for channel 1
2D	4	I	Input for channel 2
2Q	5	O	Output for channel 2
3Q	6	O	Output for channel 3
3D	7	I	Input for channel 3
4D	8	I	Input for channel 4
4Q	9	O	Output for channel 4
GND	10	G	Ground
LE	11	I	Latch enable
5Q	12	O	Output for channel 5
5D	13	I	Input for channel 5
6D	14	I	Input for channel 6
6Q	15	O	Output for channel 6
7Q	16	O	Output for channel 7
7D	17	I	Input for channel 7
8D	18	I	Input for channel 8
8Q	19	O	Output for channel 8
V_{CC}	20	P	Postive supply

(1) Signal Types: I = Input, O = Output, G = Ground, P = Power.

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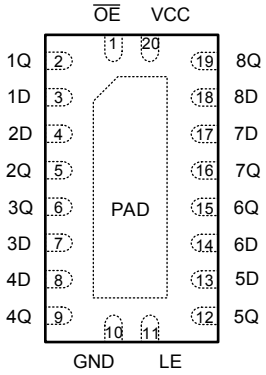


Figure 4-3. SN74AHCT373 RKS Package (Top View)

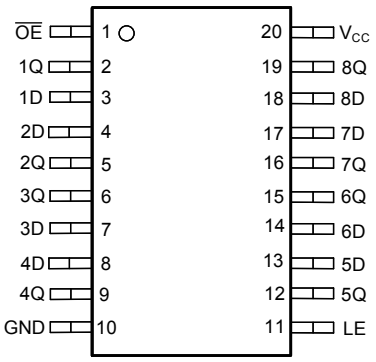


Figure 4-4. SN74AHCT373 PW , DW , NS , N , DB , DGS Package (Top View)

Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
$\overline{OE}$	1	I	Output enable, active low
1Q	2	O	Output for channel 1
1D	3	I	Input for channel 1
2D	4	I	Input for channel 2
2Q	5	O	Output for channel 2
3Q	6	O	Output for channel 3
3D	7	I	Input for channel 3
4D	8	I	Input for channel 4
4Q	9	O	Output for channel 4
GND	10	G	Ground
LE	11	I	Latch enable
5Q	12	O	Output for channel 5
5D	13	I	Input for channel 5
6D	14	I	Input for channel 6
6Q	15	O	Output for channel 6
7Q	16	O	Output for channel 7
7D	17	I	Input for channel 7
8D	18	I	Input for channel 8
8Q	19	O	Output for channel 8
V_{CC}	20	P	Postive supply
Thermal Pad[2]		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) Signal Types: I = Input, O = Output, G = Ground, P = Power.
(2) RKS package only.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range(2)		–0.5	7	V
V_O	Output voltage range(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{CC}		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±75	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			Value	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		SN54AHCT373		SN74AHCT373		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

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5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC(1)						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
DGS (VSSOP)	20	131.6	69.5	86.7	10.9	85.9	N/A	°C/W
PW (TSSOP)	20	116.8	-	-	-	-	N/A	°C/W
RKS (VQFN)	20	90.4	92.2	63.4	29	63.5	41.3	°C/W
DW (SOIC)	20	58	-	-	-	-	N/A	°C/W
DB (SSOP)	20	70	-	-	-	-	N/A	°C/W
N (PDIP)	20	69	-	-	-	-	N/A	°C/W
NS (SOP)	20	60	-	-	-	-	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT373		SN74AHCT373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50µA	4.5V	4.4	4.5		4.4		4.4		V
	I_{OH} = −8mA		3.94			3.8		3.8		
V_{OL}	I_{OL} = 50µA	4.5V			0.1		0.1		0.1	V
	I_{OL} = 8mA				0.36		0.44		0.44	
I_{OZ}	V_O = V_{CC} or GND	5.5V			± 0.25		± 2.5		± 2.5	µA
I_I	V_I = 5.5V or GND	0V to 5.5V			±0.1		± 1 (1)		±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5V			4		40		40	µA
ΔI_{CC}†	One input at 3.4V,Other inputs at V_{CC} or GND	5.5V			1.35		1.5		1.5	mA
C_i	V_I = V_{CC} or GND	5V		4	10				10	pF
C_o	V_O = V_{CC} or GND	5V		9						pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0V.

5.6 Timing Requirements, V_{CC} = 5V ±0.5V

over recommended operating free-air temperature range (unless otherwise noted) (see Parameter Measurement Information)

PARAMETER		T_A = 25°C		SN54AHCT373		SN74AHCT373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, $\overline{LE}$ high	6.5		6.5		6.5		ns
t_{su}	Setup time, data before $\overline{LE}$↓	1.5		1.5		1.5		ns
t_h	Hold time, data after $\overline{LE}$↓	3.5		3.5		3.5		ns

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5.7 Switching Characteristics, V_{CC} = 5V ±0.5V

over recommended operating free-air temperature range (unless otherwise noted) (see Parameter Measurement Information)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHCT373		SN74AHCT373		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	C_L = 15pF		5.1(1)	8.5(1)	1(1)	9.5(1)	1	9.5	ns
t_{PHL}					5.1(1)	8.5(1)	1(1)	9.5(1)	1	9.5	
t_{PLH}	LE	Q	C_L = 15pF		7.7(1)	12.3(1)	1(1)	13.5(1)	1	13.5	ns
t_{PHL}					7.7(1)	12.3(1)	1(1)	13.5(1)	1	13.5	
t_{PZH}	$\overline{OE}$	Q	C_L = 15pF		6.3(1)	10.9(1)	1(1)	12.5(1)	1	12.5	ns
t_{PZL}					6.3(1)	10.9(1)	1(1)	12.5(1)	1	12.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 15pF		6(1)	10.2(1)	1(1)	11(1)	1	11	ns
t_{PLZ}					6(1)	10.2(1)	1(1)	11(1)	1	11	
t_{PLH}	D	Q	C_L = 50pF		5.9	9.5	1	10.5	1	10.5	ns
t_{PHL}					5.9	9.5	1	10.5	1	10.5	
t_{PLH}	LE	Q	C_L = 50pF		8.5	13.3	1	14.5	1	14.5	ns
t_{PHL}					8.5	13.3	1	14.5	1	14.5	
t_{PZH}	$\overline{OE}$	Q	C_L = 50pF		7.1	11.9	1	13.5	1	13.5	ns
t_{PZL}					7.1	11.9	1	13.5	1	13.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50pF		6.8	11.2	1	12	1	12	ns
t_{PLZ}					6.8	11.2	1	12	1	12	
$t_{sk(o)}$			C_L = 50pF			1(2)				1	ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

5.8 Noise Characteristics

V_{CC} = 5V, C_L = 50pF, T_A = 25°C(1)

PARAMETER		SN74AHCT373			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	1.2	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.8	–1.2	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.1			V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

(1) Characteristics are for surface-mount packages only.

5.9 Operating Characteristics

V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1MHz	17	pF

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5.10 Typical Characteristics

T_A = 25°C (unless otherwise noted)

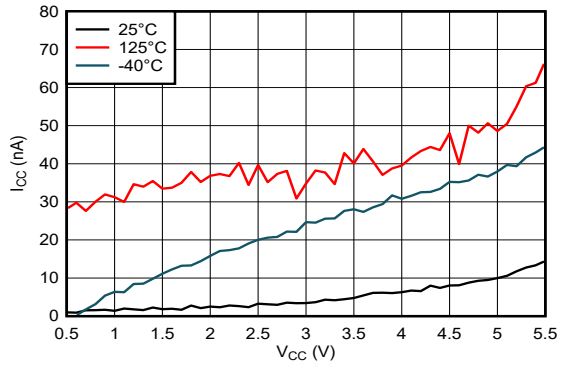


Figure 5-1. Supply Current Across Supply Voltage

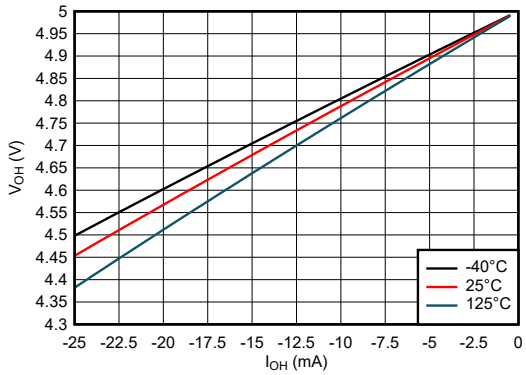


Figure 5-2. Output Voltage vs Current in HIGH State; 5V Supply

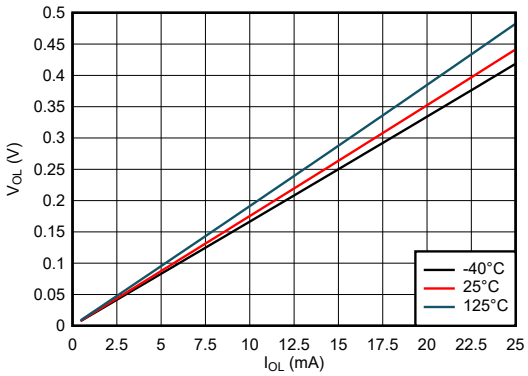


Figure 5-3. Output Voltage vs Current in LOW State; 5V Supply

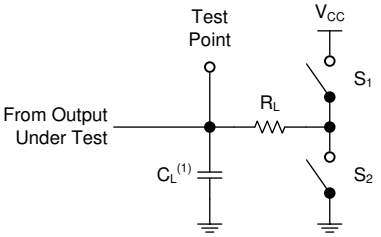
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6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t < 3ns .

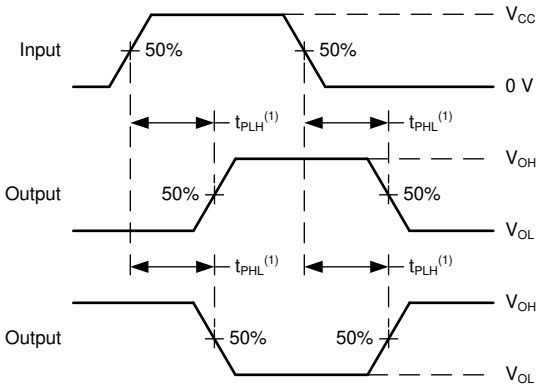
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for 3-State Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-2. Voltage Waveforms Propagation Delays

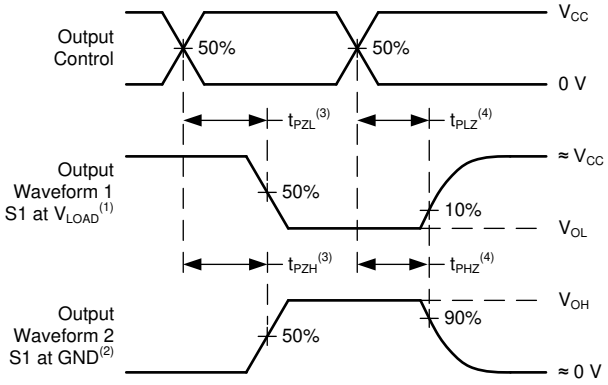
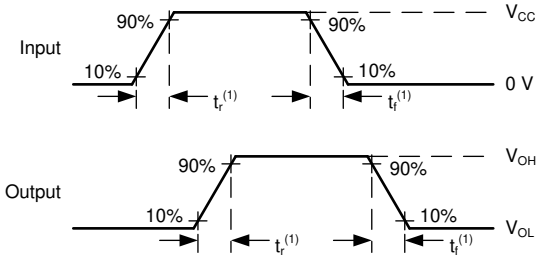


Figure 6-3. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

Figure 6-4. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Overview

The SNx4AHCT373 contains eight D-type latches. All channels share a latch enable (LE) and output enable ($\overline{OE}$) input.

When the latch is enabled (LE is high), data is allowed to pass through from the D inputs to the Q outputs.

When the latch is disabled (LE is low), the Q outputs hold the last state they had regardless of changes at the D inputs.

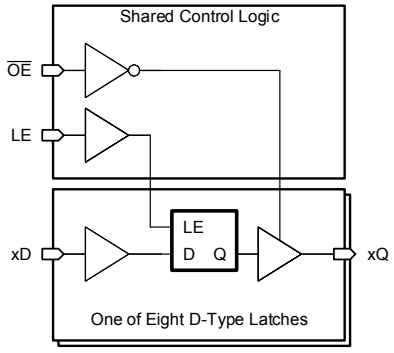
If the latch enable (LE) input is held low during startup, the output state of all channels is unknown until the latch enable (LE) input is driven high with valid input signals at all data (D) inputs.

When the outputs are enabled ($\overline{OE}$ is low), the outputs are actively driving low or high.

When the outputs are disabled ($\overline{OE}$ is high), the outputs are set into the high-impedance state.

The active low output enable ($\overline{OE}$) does not have any impact on the stored state in the latches.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

7.3.2 TTL-Compatible CMOS Inputs

This device includes TTL-compatible CMOS inputs. These inputs are specifically designed to interface with TTL logic devices by having a reduced input voltage threshold.

TTL-compatible CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

TTL-compatible CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the *Implications of Slow or Floating CMOS Inputs* application report.

Do not leave TTL-compatible CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10kΩ resistor is recommended and typically will meet all requirements.

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7.3.3 Clamp Diode Structure

As Figure 7-1 shows, the outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

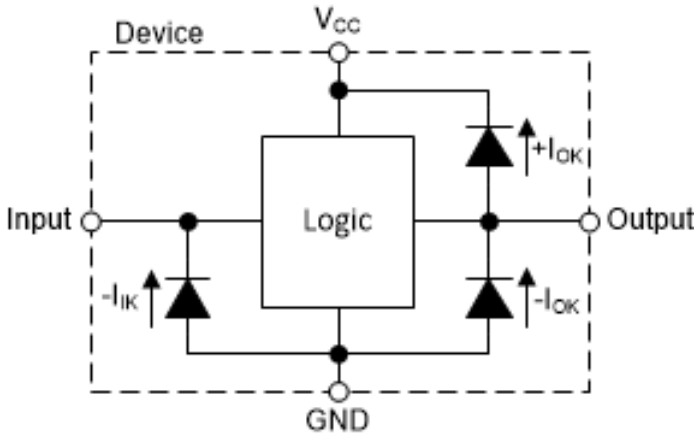


Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

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7.4 Device Functional Modes

Table 7-1. Function Table

INPUTS[1]			OUTPUT[2]
$\overline{OE}$	LE	D	Q
L	H	L	L
L	H	H	H
L	L	X	Q_0 [3]
H	X	X	Z

(1) L = input low, H = input high, ↑ = input transitioning from low to high, ↓ = input transitioning from high to low, X = don't care
(2) L = output low, H = output high, Q_0 = previous state, Z = high impedance
(3) At startup, Q_0 is unknown

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, the SNx4AHCT373 is used to control an 8-bit data bus.

Outputs can be held in the high-impedance state, held in the last known state, or change together with the data inputs, depending on the control inputs at LE and $\overline{OE}$ coming from the bus controller.

8.2 Typical Application

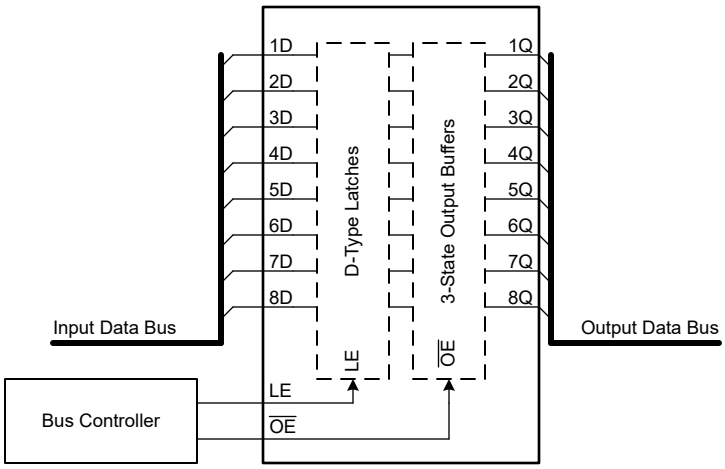


Figure 8-1. Typical Application Block Diagram

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8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Electrical Characteristics*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SNx4AHCT373 plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SNx4AHCT373 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SNx4AHCT373 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SNx4AHCT373 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in the *CMOS Power Consumption and Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

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8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SNx4AHCT373 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The SNx4AHCT373 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Electrical Characteristics* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

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8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Verify that the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SNx4AHCT373 to one or more of the receiving devices.
3. Verify that the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$)Ω. Doing this prevents the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the *CMOS Power Consumption and Cpd Calculation* application note.

8.2.3 Application Curves

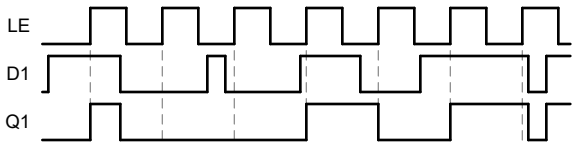


Figure 8-2. Application Timing Diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance.

A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - Parallel traces must be separated by at least 3x dielectric thickness
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer each signal that must branch separately

8.4.2 Layout Example

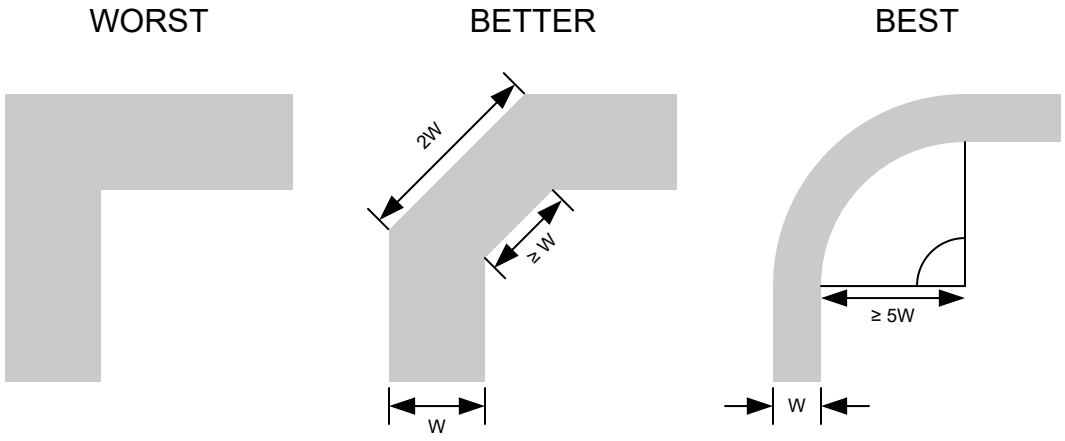


Figure 8-3. Example Trace Corners for Improved Signal Integrity

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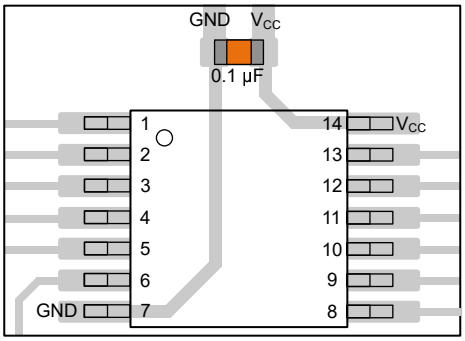


Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

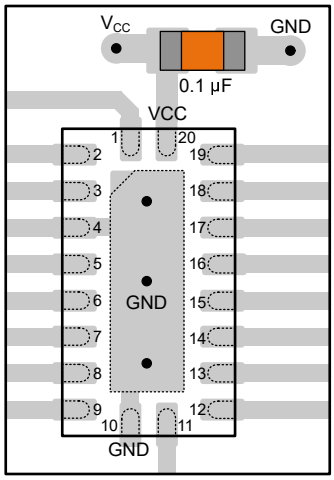


Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

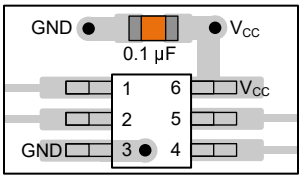


Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

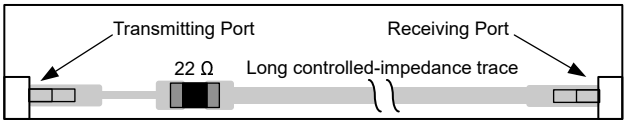


Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision O (August 2024) to Revision P (July 2025)	Page
• Added RKS and DGS packages	6

Changes from Revision N (August 2023) to Revision O (August 2024)	Page
• Added package size to *Device Information* table	2
• Updated RθJA values: PW = 83 to 116.8, all values in °C/W	6

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Changes from Revision M (July 2023) to Revision N (August 2023) **Page**

- Added *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Device Functional Modes*, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 2

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9686701Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9686701Q2A SNJ54AHCT373FK
5962-9686701QRA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9686701QRA SNJ54AHCT373J
5962-9686701QSA	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9686701QSA SNJ54AHCT373W
SN74AHCT373DBR	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB373
SN74AHCT373DBR.A	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB373
SN74AHCT373DGSR	Active	Production	VSSOP (DGS) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB273
SN74AHCT373DW	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	-40 to 85	AHCT373
SN74AHCT373DWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT373
SN74AHCT373DWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT373
SN74AHCT373N	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AHCT373N
SN74AHCT373N.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AHCT373N
SN74AHCT373NSR	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT373
SN74AHCT373NSR.A	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT373
SN74AHCT373PW	Obsolete	Production	TSSOP (PW) | 20	-	-	Call TI	Call TI	-40 to 85	HB373
SN74AHCT373PWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB373
SN74AHCT373PWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB373
SN74AHCT373RKSR	Active	Production	VQFN (RKS) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT373
SNJ54AHCT373FK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9686701Q2A SNJ54AHCT373FK
SNJ54AHCT373FK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9686701Q2A SNJ54AHCT373FK

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54AHCT373J	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9686701QR A SNJ54AHCT373J
SNJ54AHCT373J.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9686701QR A SNJ54AHCT373J
SNJ54AHCT373W	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9686701QS A SNJ54AHCT373W
SNJ54AHCT373W.A	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9686701QS A SNJ54AHCT373W

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AHCT373, SN74AHCT373 :

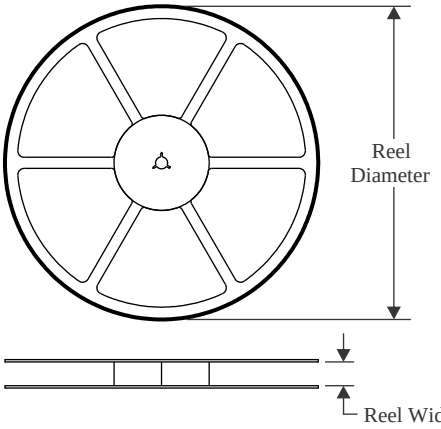
- Catalog : SN74AHCT373
- Automotive : SN74AHCT373-Q1, SN74AHCT373-Q1
- Military : SN54AHCT373

NOTE: Qualified Version Definitions:

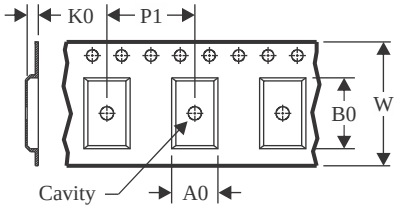
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

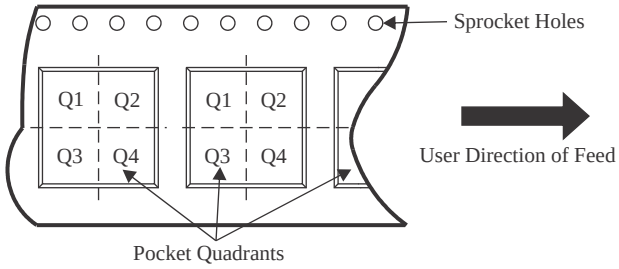


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

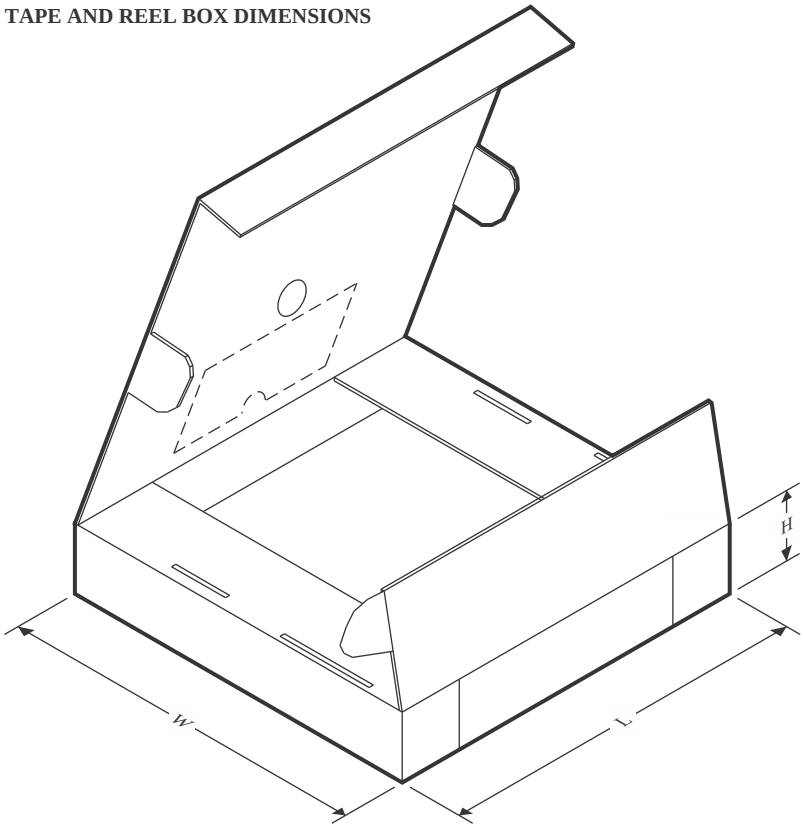
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT373DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHCT373DGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74AHCT373DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHCT373NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AHCT373PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AHCT373RKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

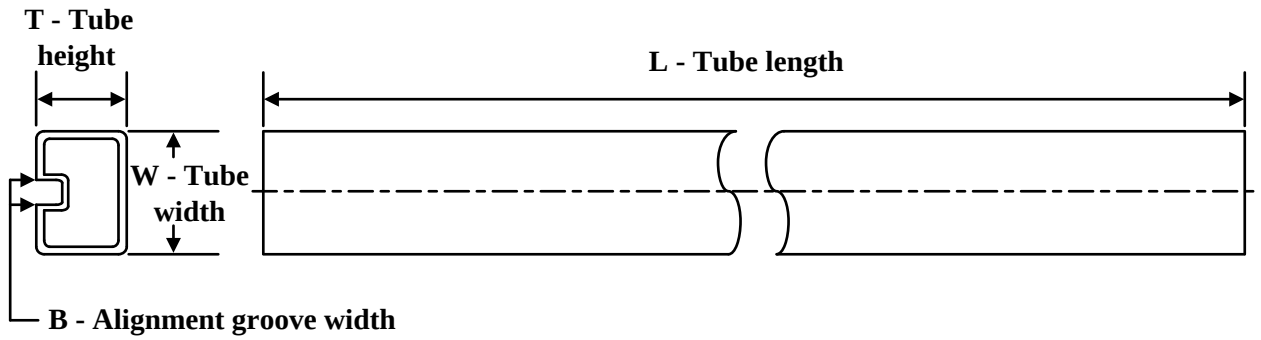
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT373DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74AHCT373DGSR	VSSOP	DGS	20	5000	353.0	353.0	32.0
SN74AHCT373DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AHCT373NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74AHCT373PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74AHCT373RKSR	VQFN	RKS	20	3000	210.0	185.0	35.0

TUBE



*All dimensions are nominal

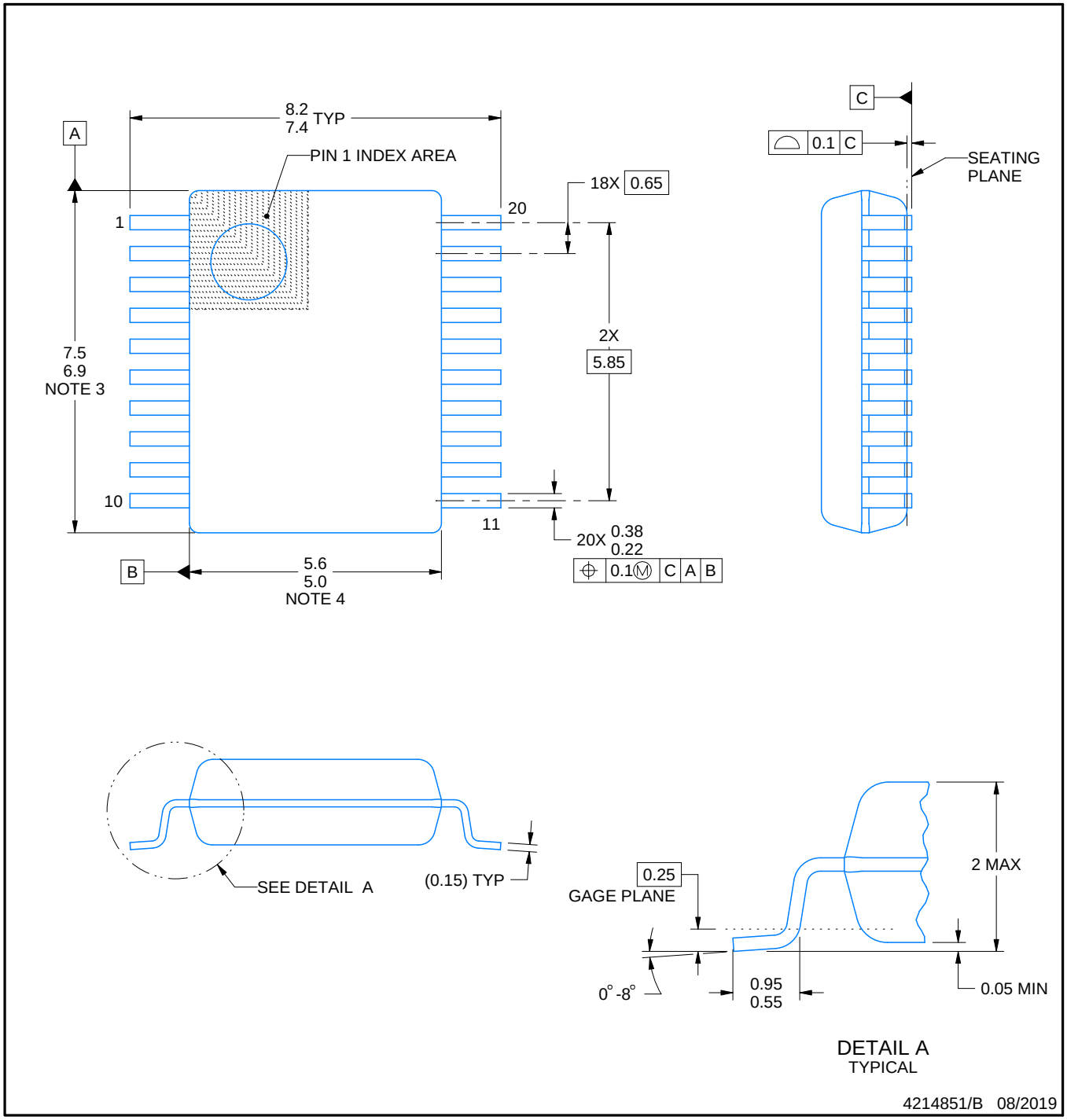
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9686701Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9686701QSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74AHCT373N	N	PDIP	20	20	506	13.97	11230	4.32
SN74AHCT373N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54AHCT373FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHCT373FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHCT373W	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54AHCT373W.A	W	CFP	20	25	506.98	26.16	6220	NA

PACKAGE OUTLINE

DB0020A

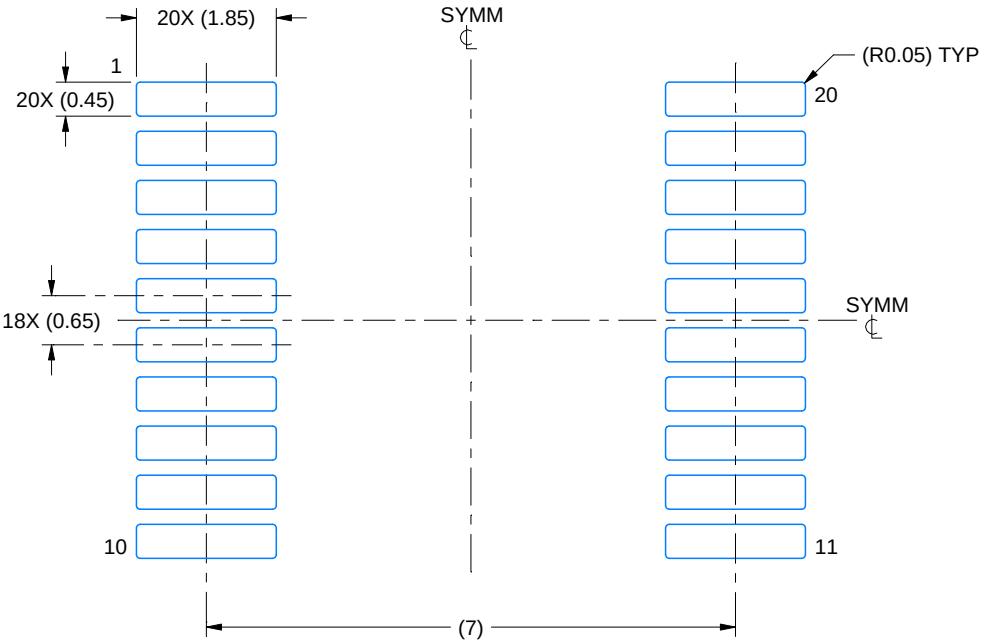
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

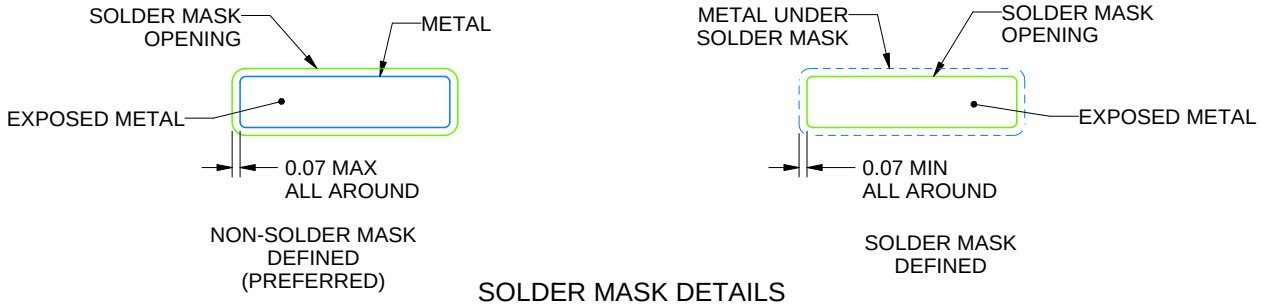


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

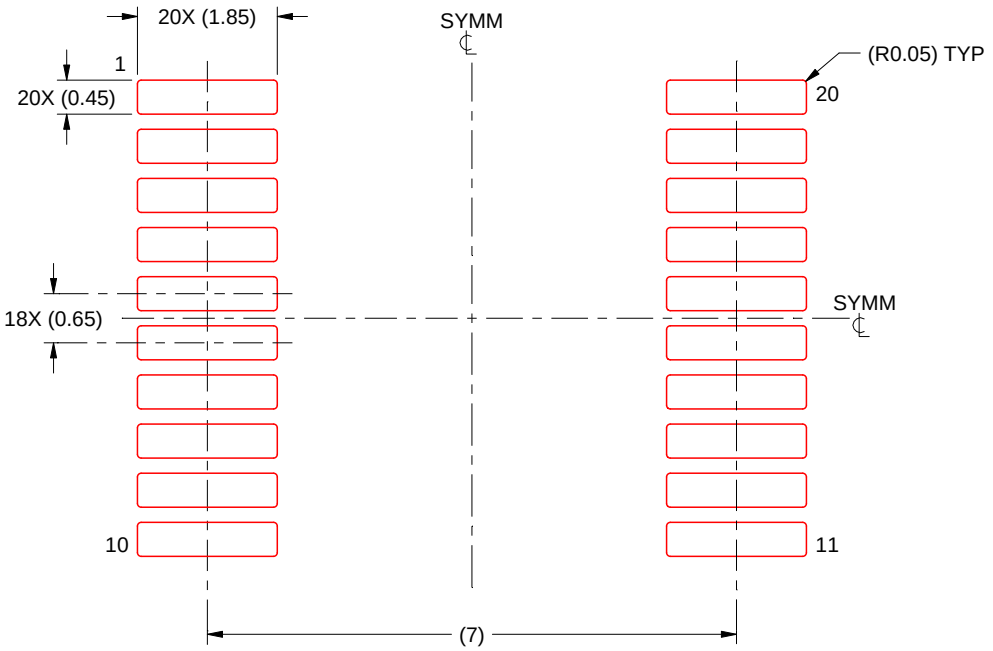
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

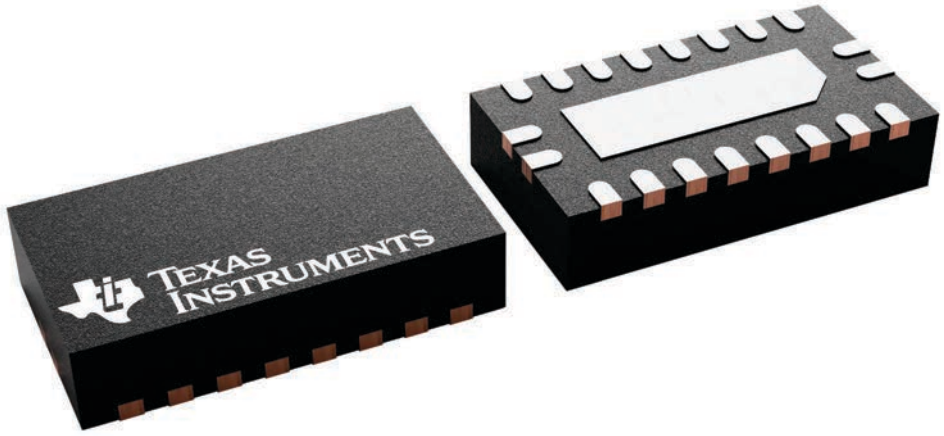
RKS 20

VQFN - 1 mm max height

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

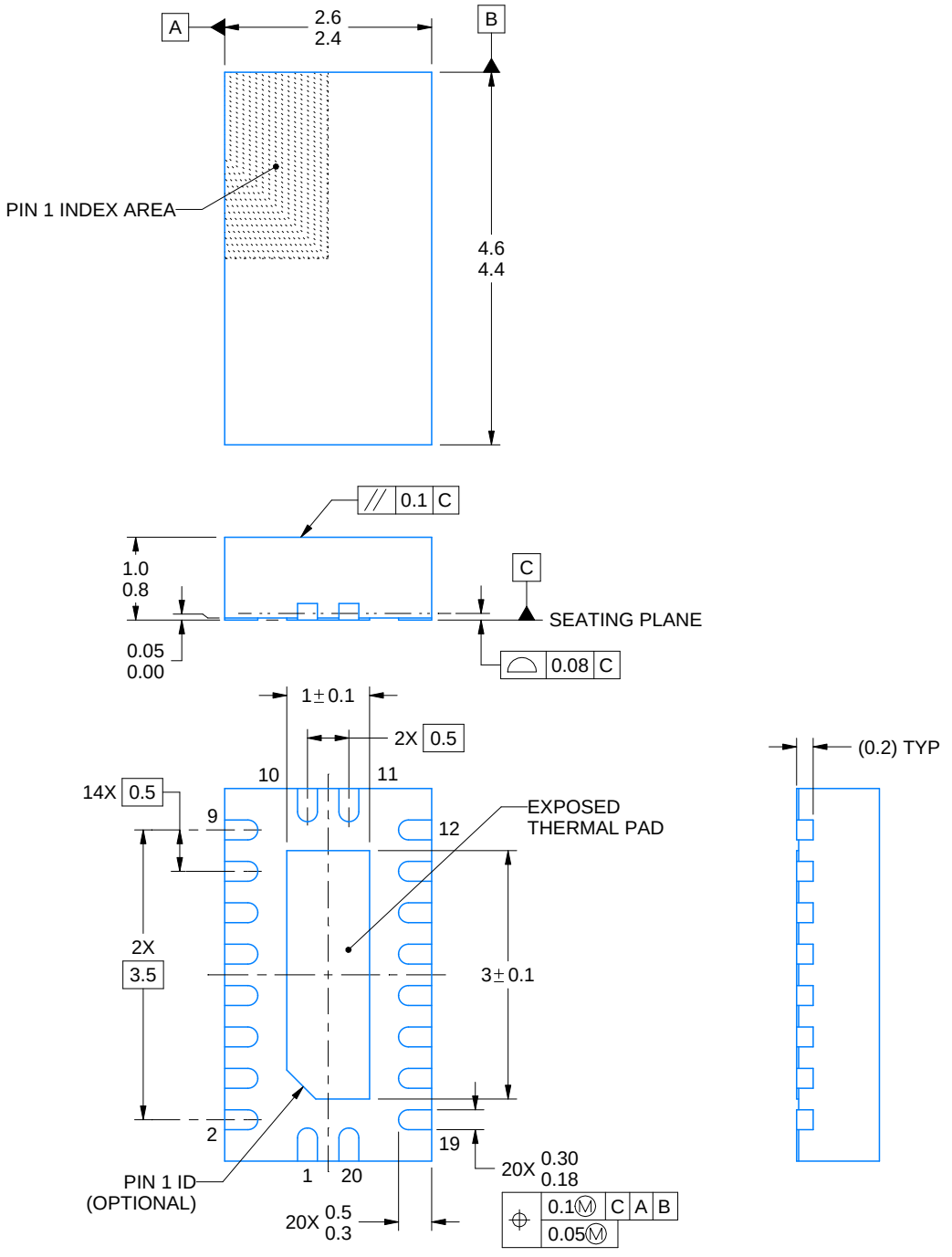


PACKAGE OUTLINE

RKS0020A

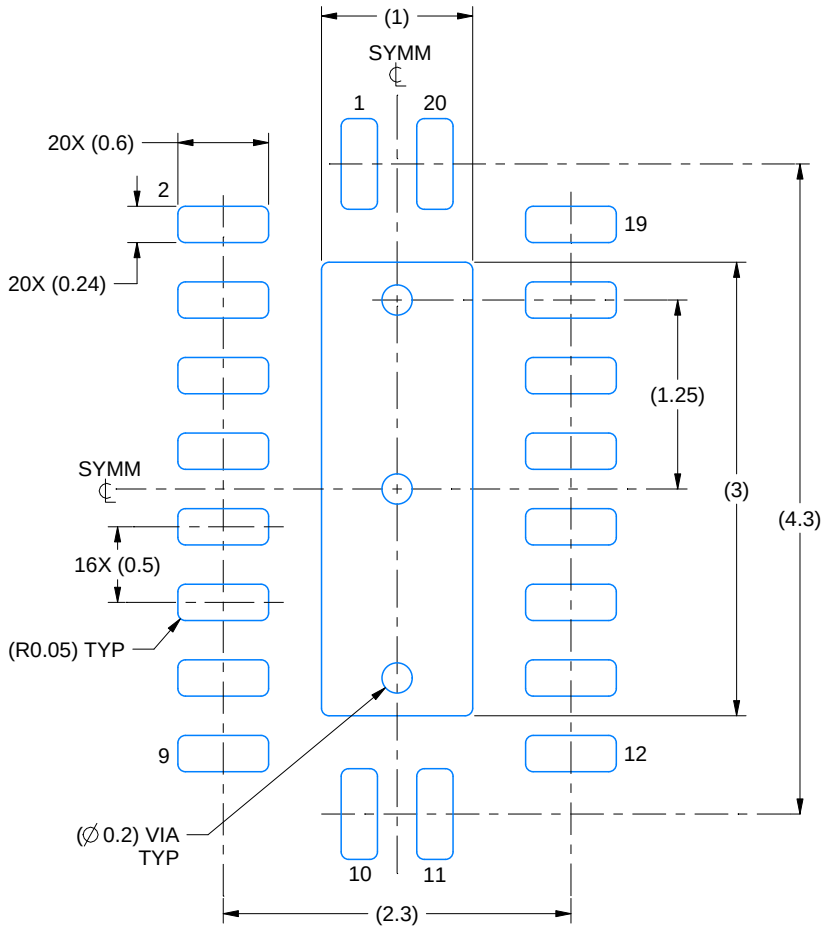
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

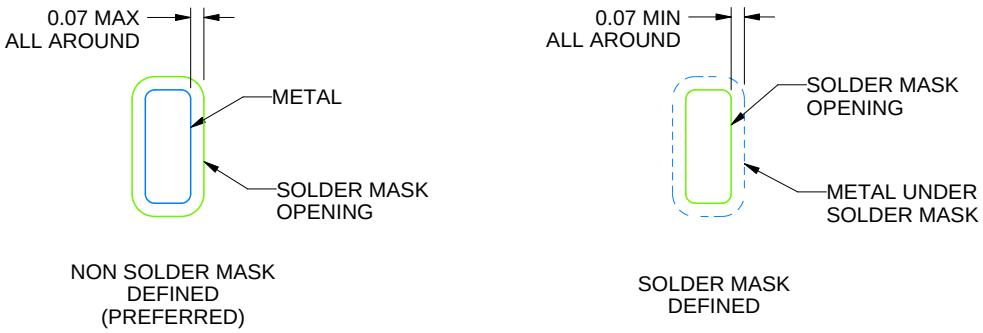


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

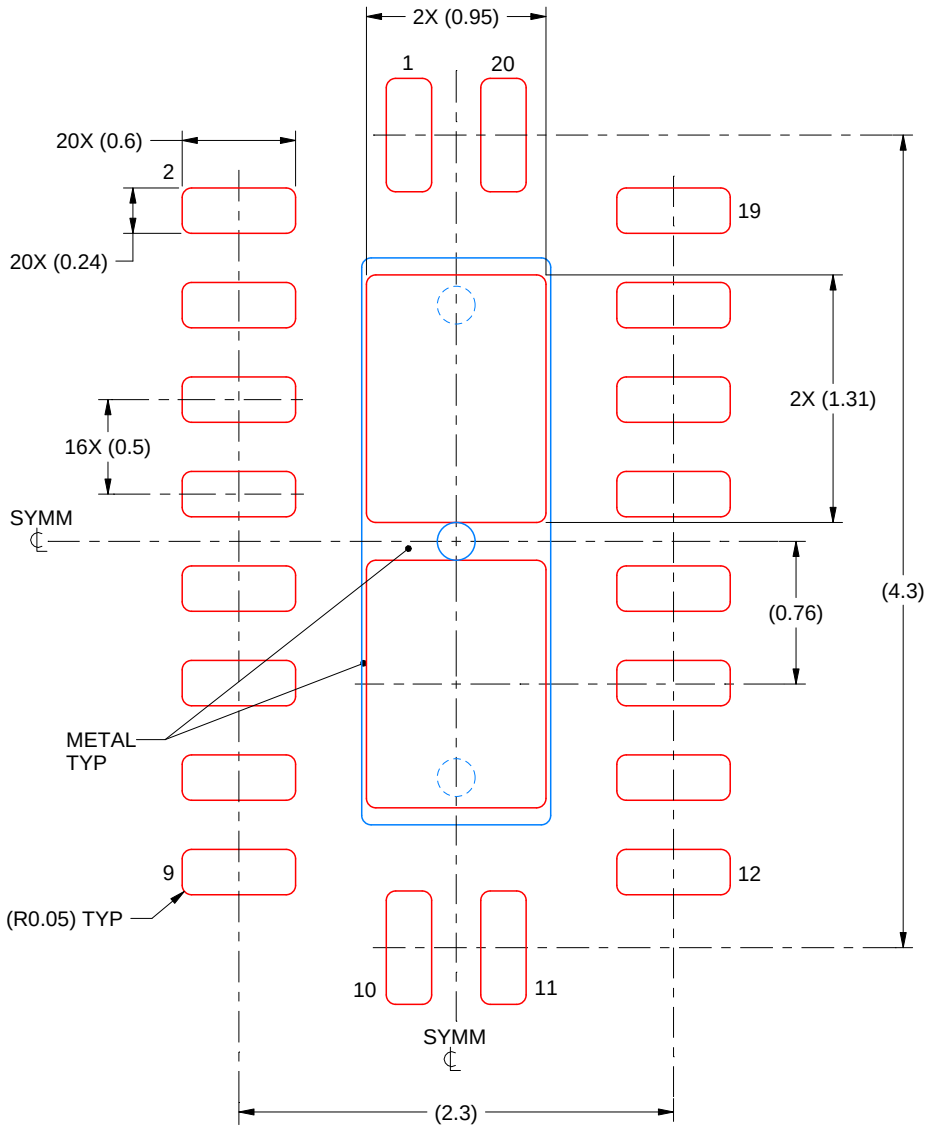


SOLDER MASK DETAILS

4222490/B 02/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222490/B 02/2021

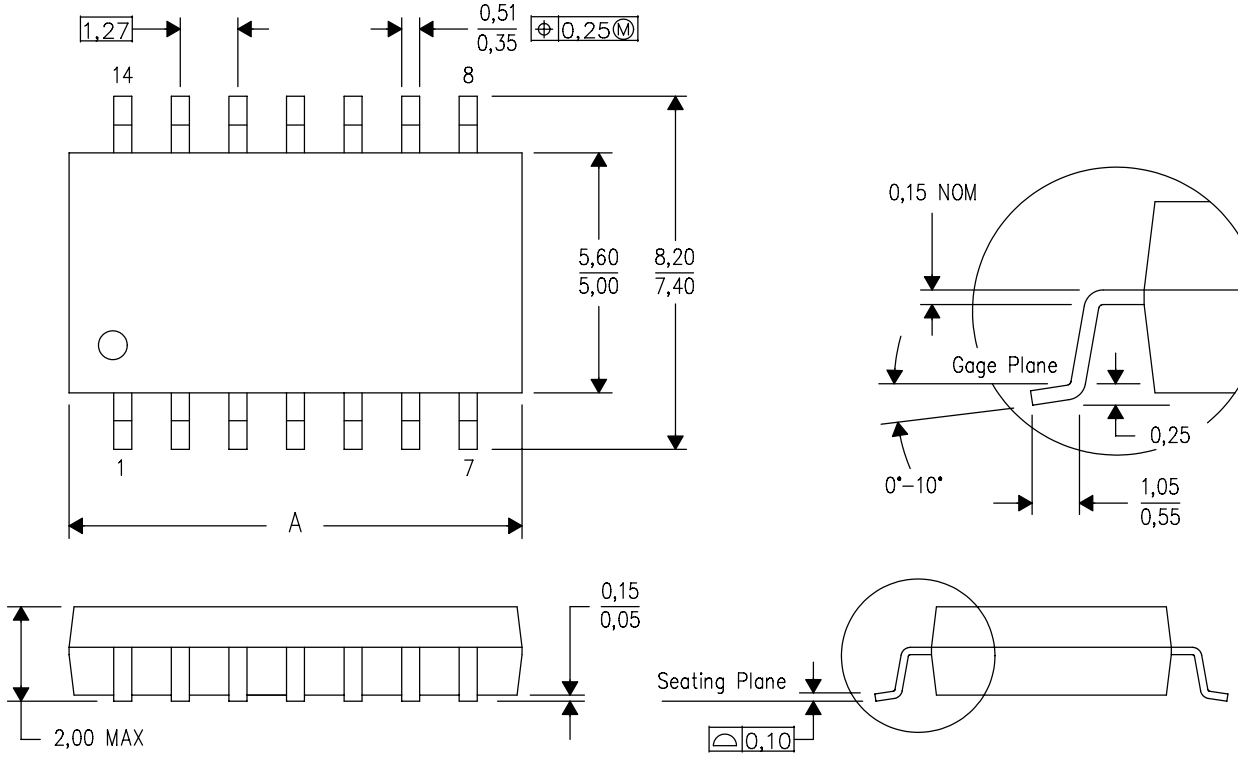
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

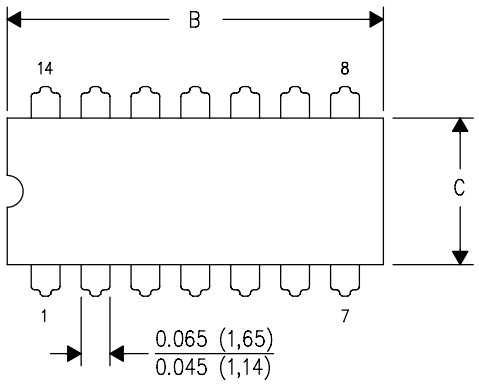
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

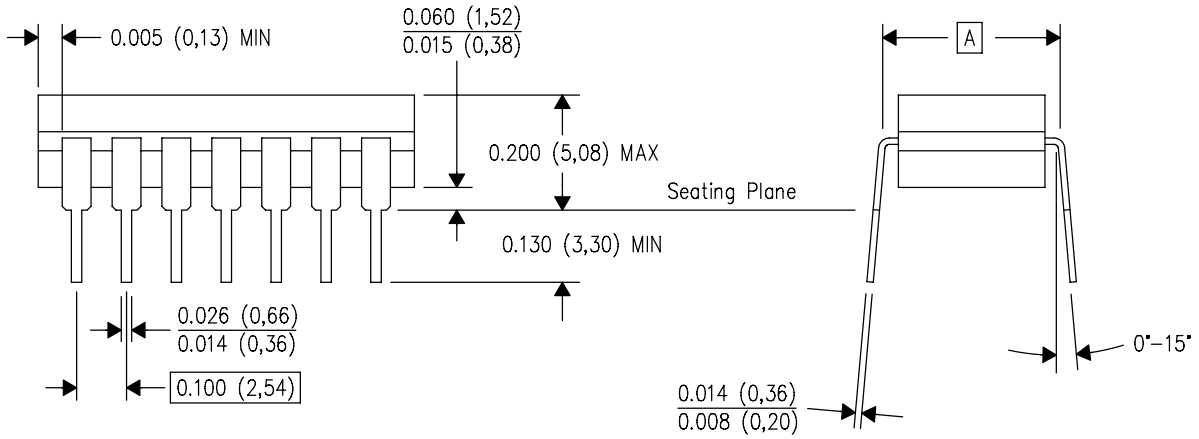
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

GENERIC PACKAGE VIEW

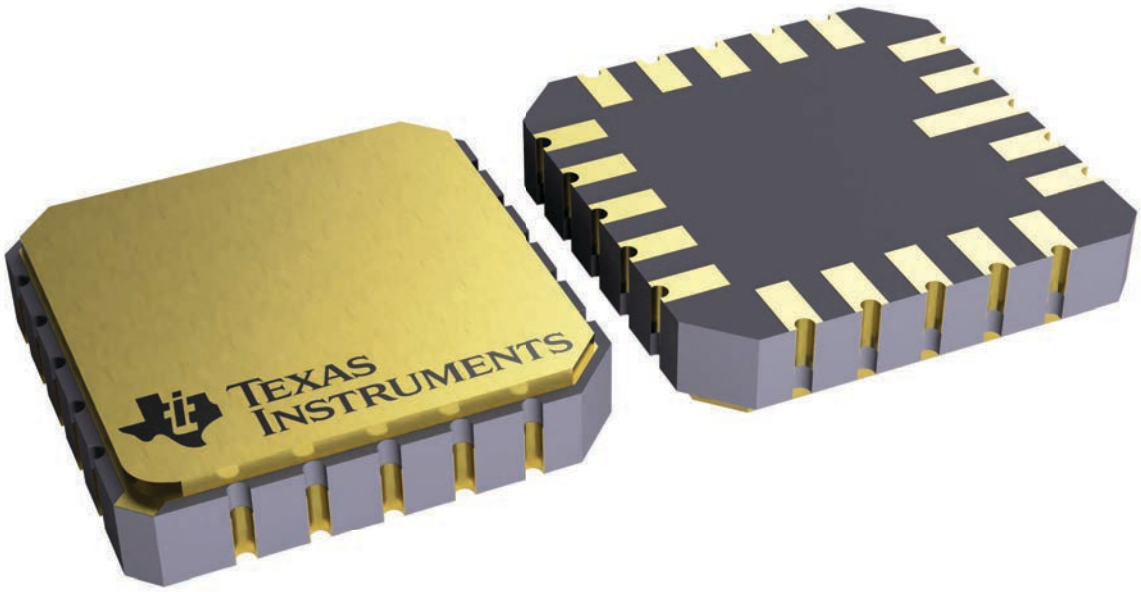
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

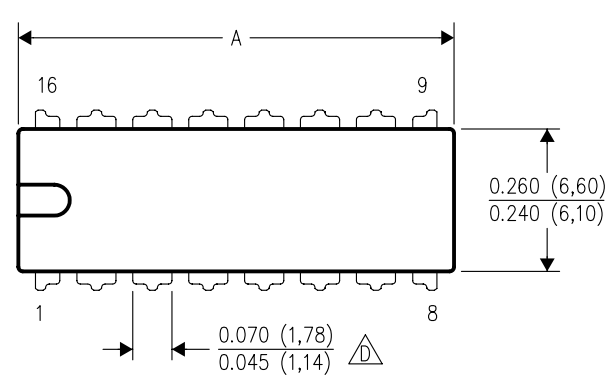


4229370VA\

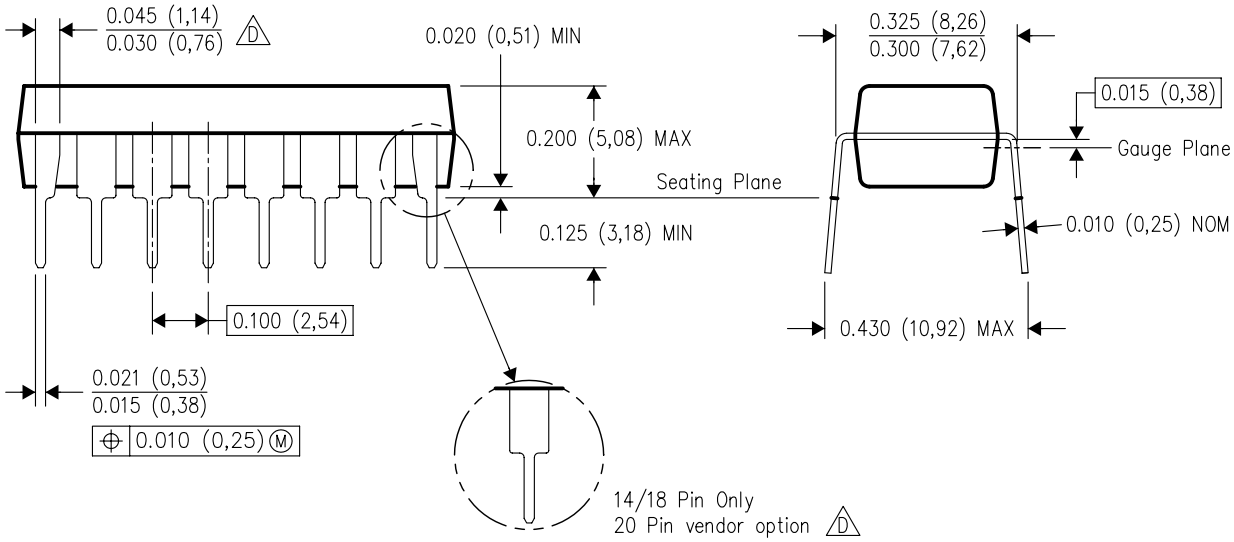
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

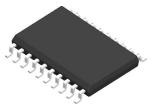


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

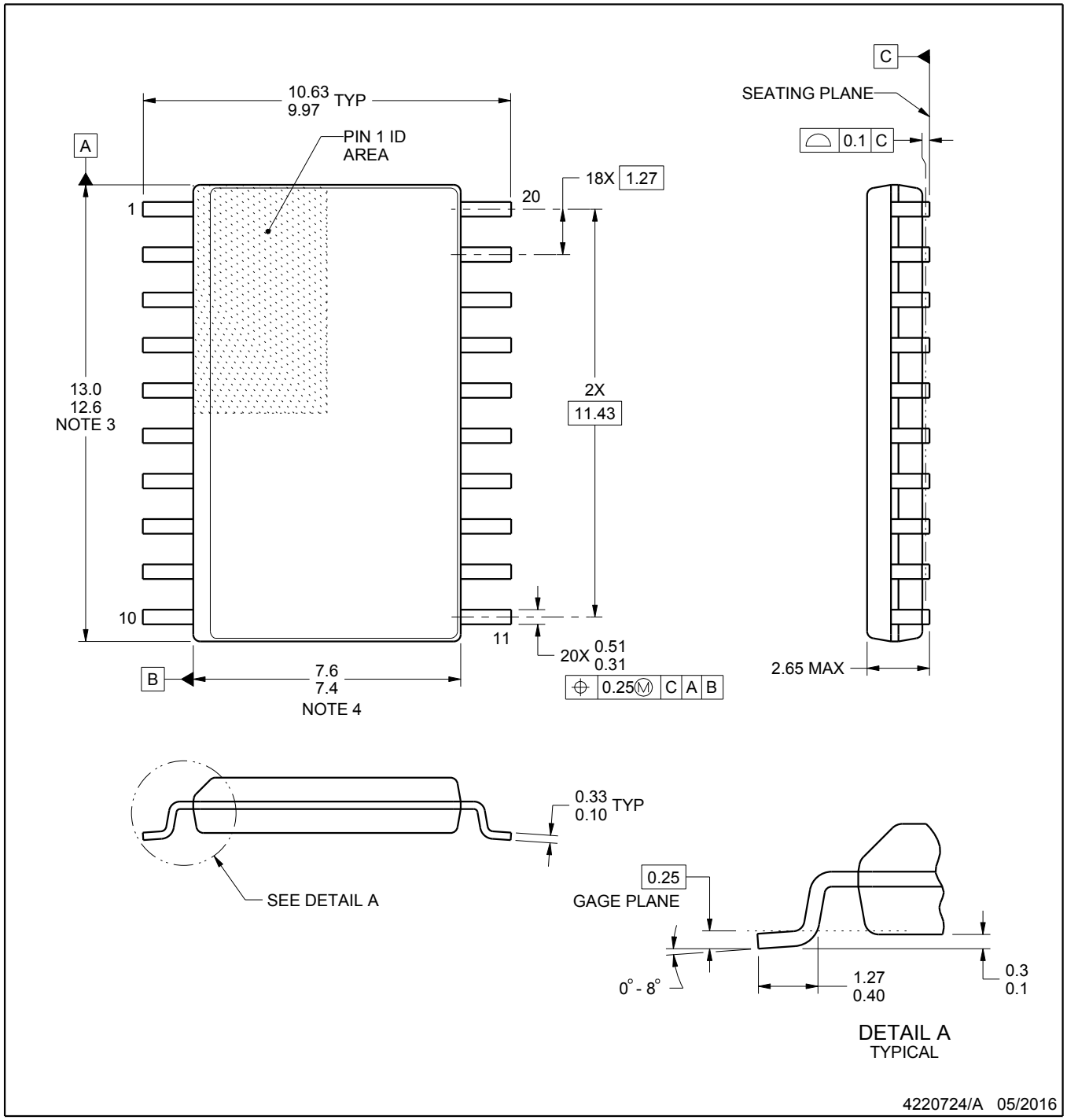


PACKAGE OUTLINE

DW0020A

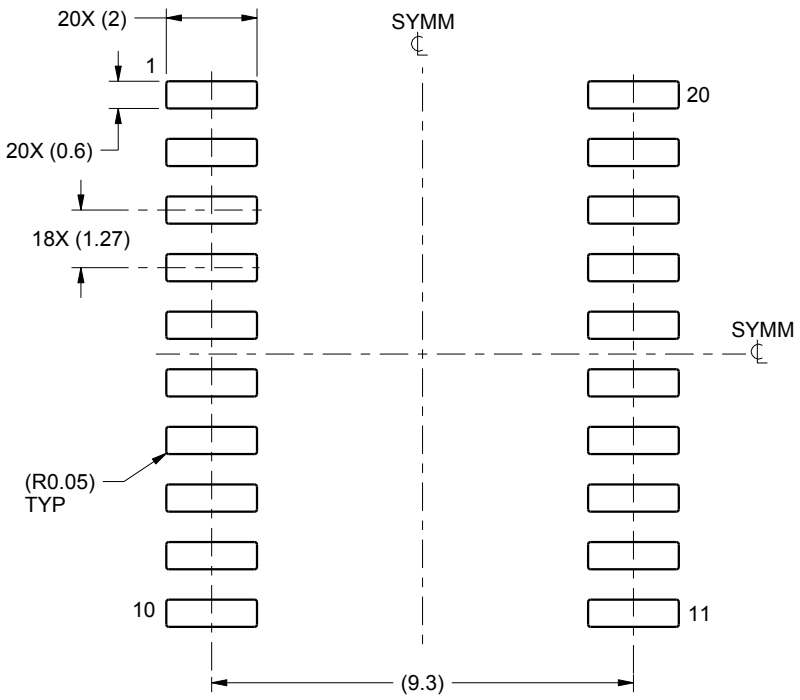
SOIC - 2.65 mm max height

SOIC

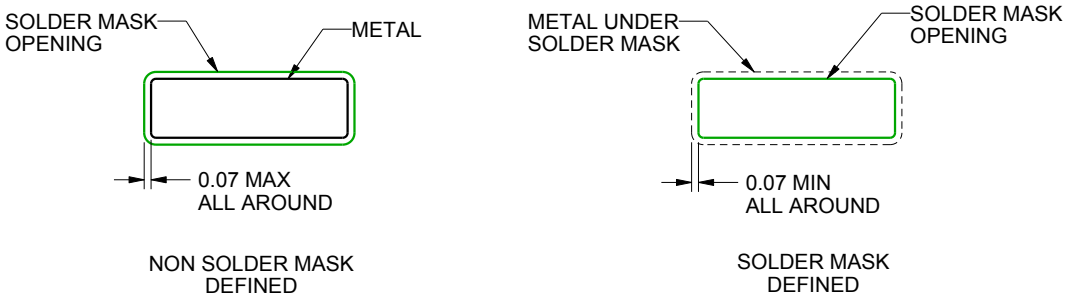


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

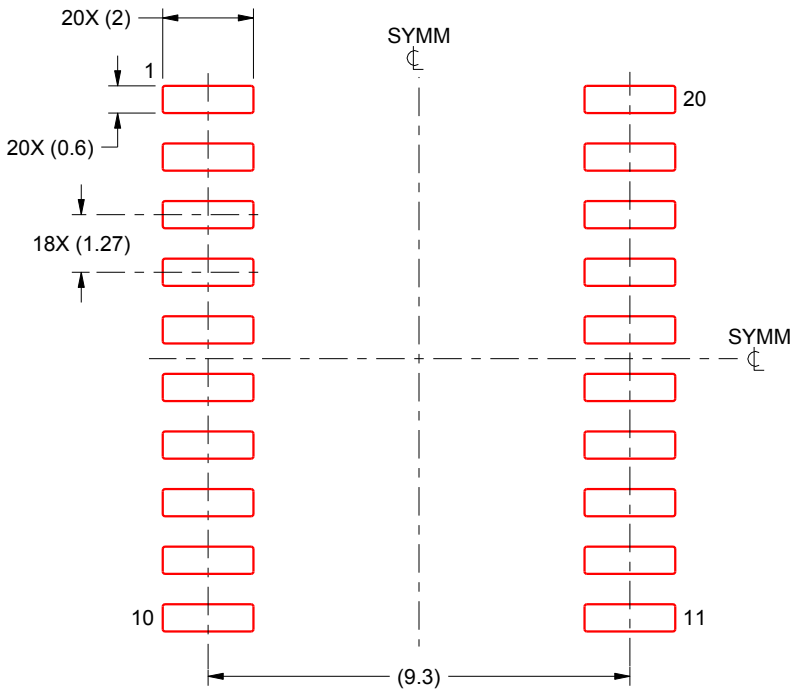


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



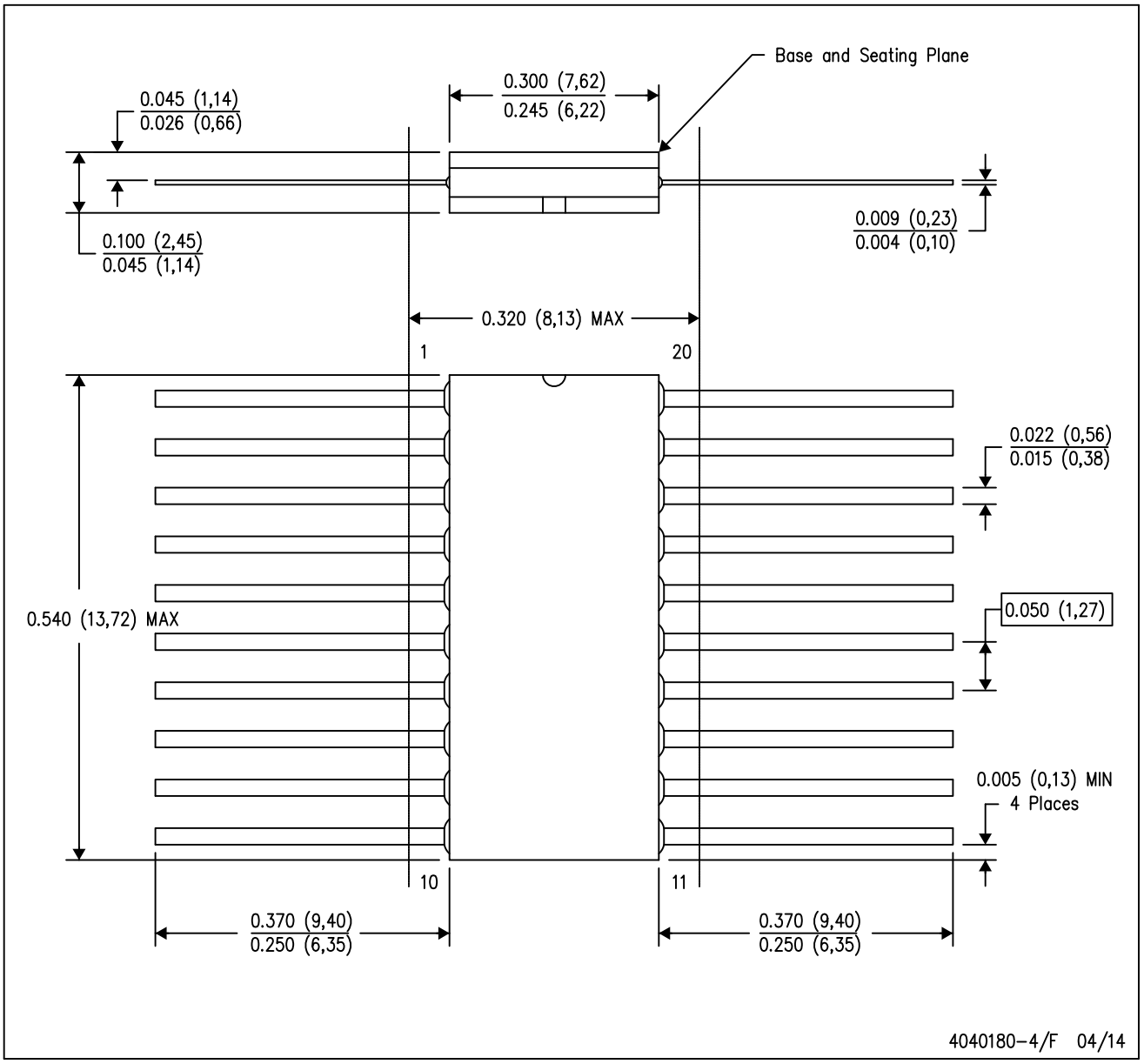
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F20) CERAMIC DUAL FLATPACK



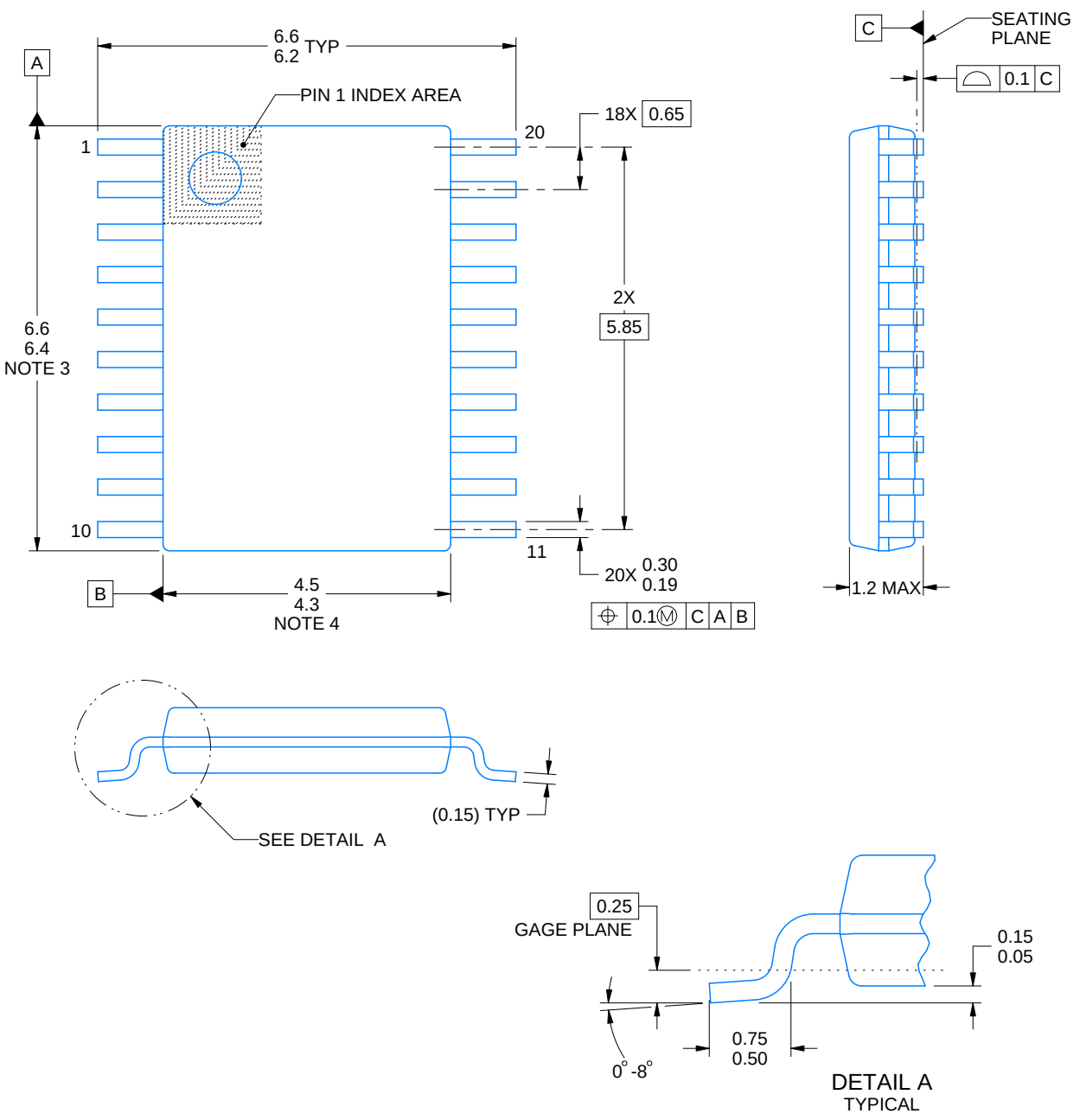
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

PACKAGE OUTLINE

PW0020A

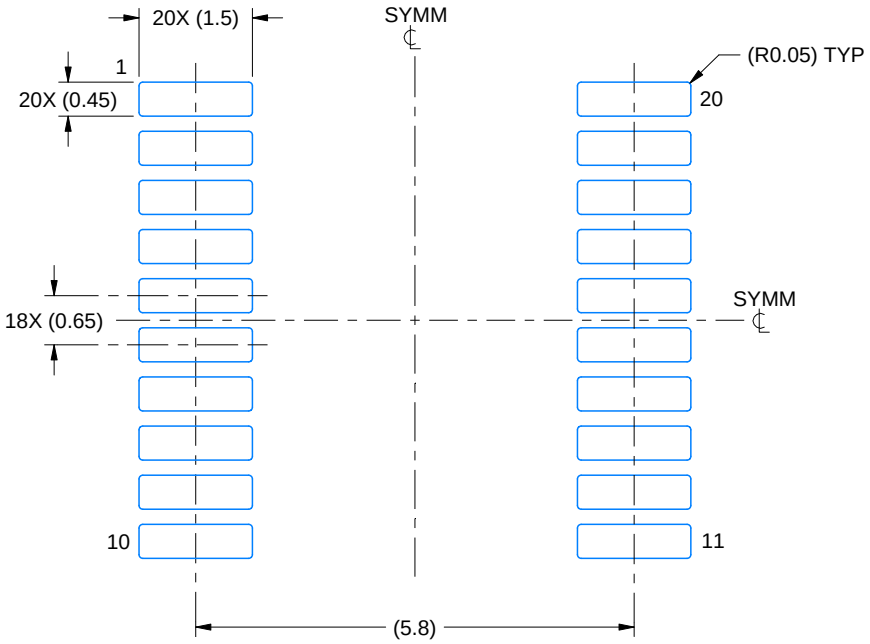
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

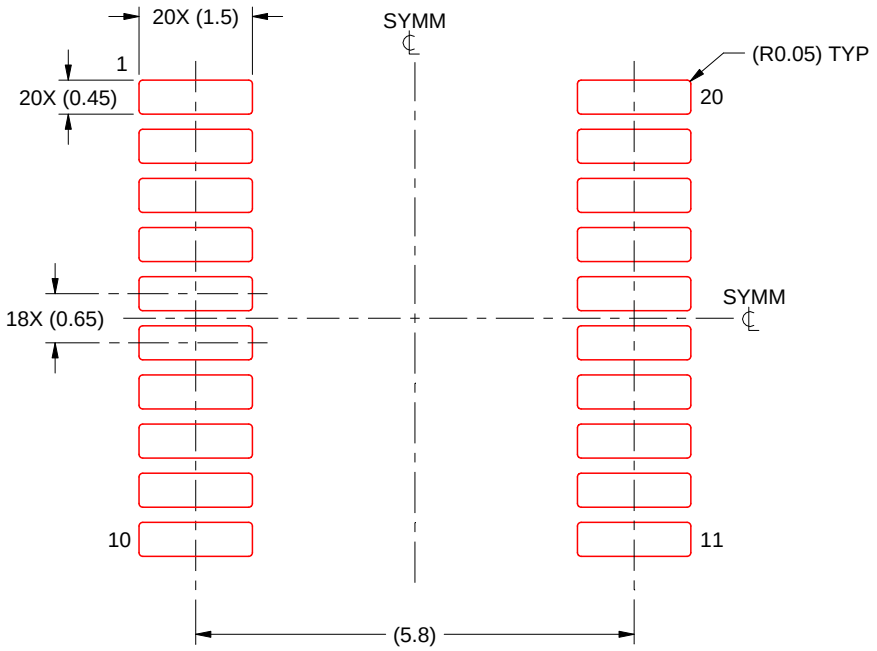


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

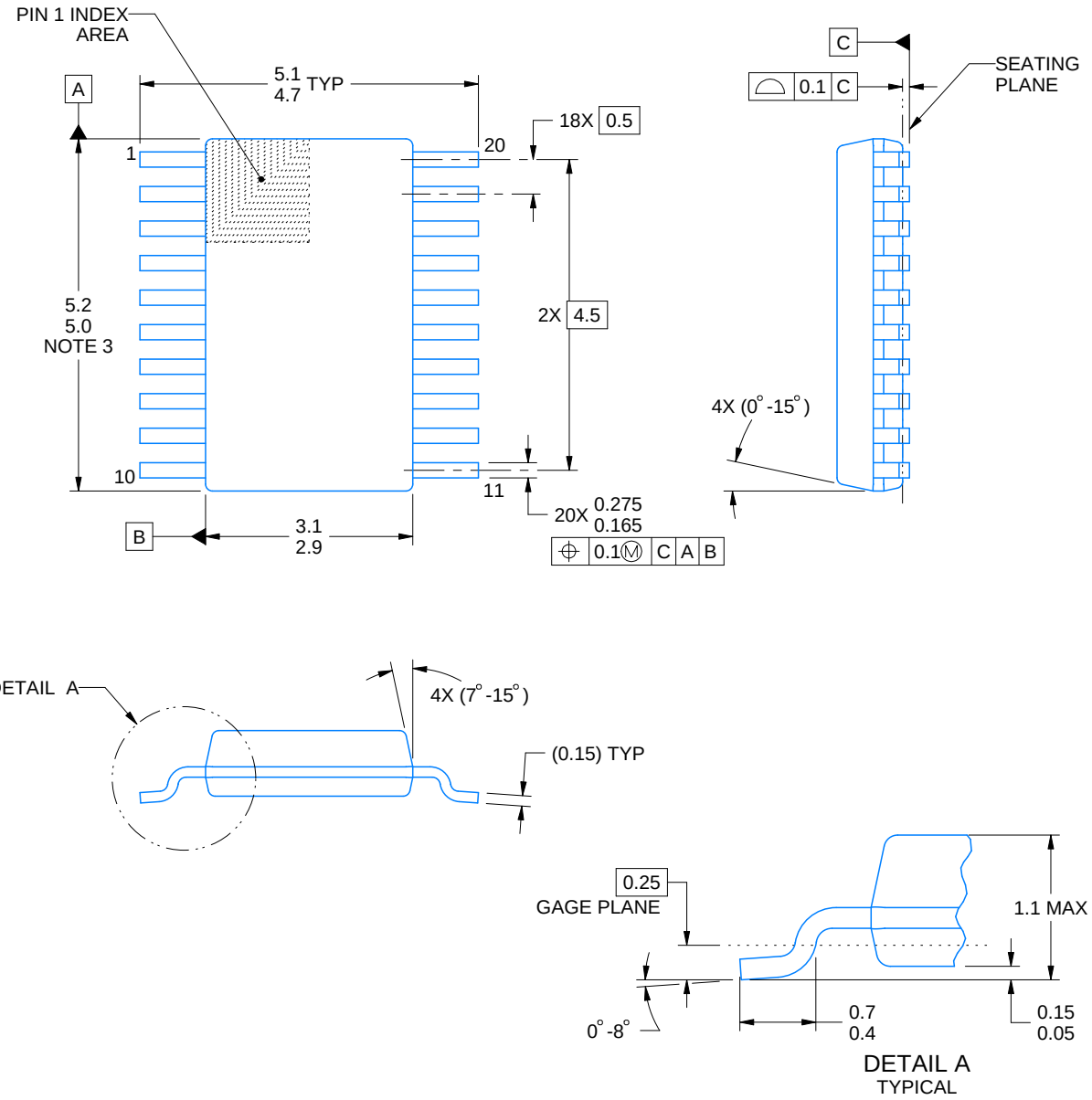
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGS0020A

VSSOP - 1.1 mm max height

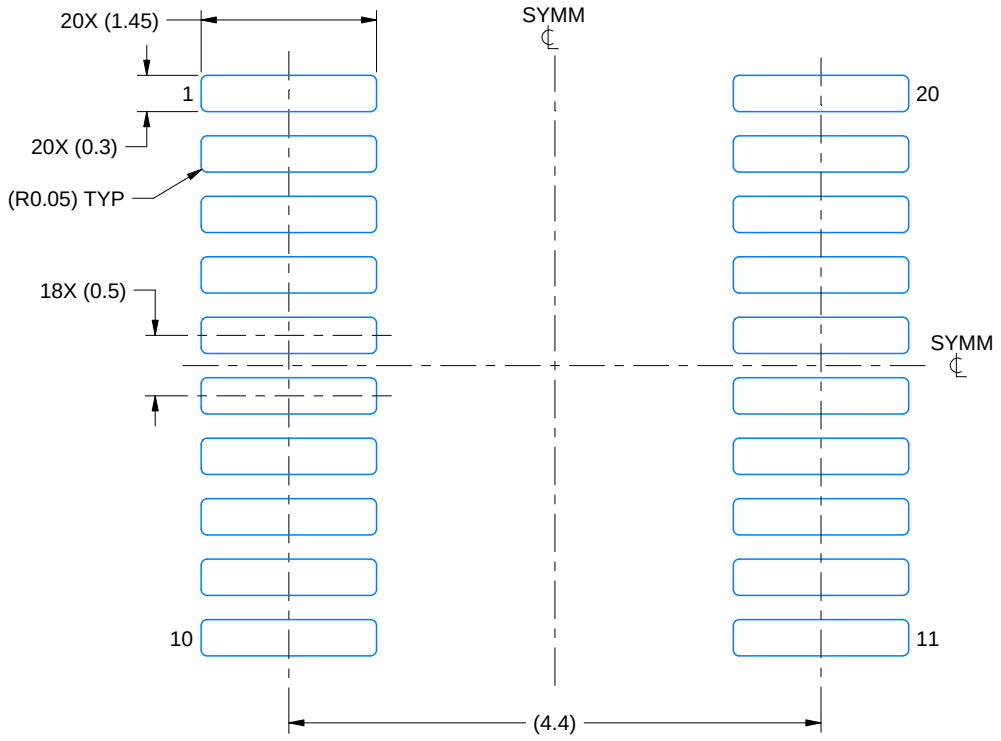
SMALL OUTLINE PACKAGE



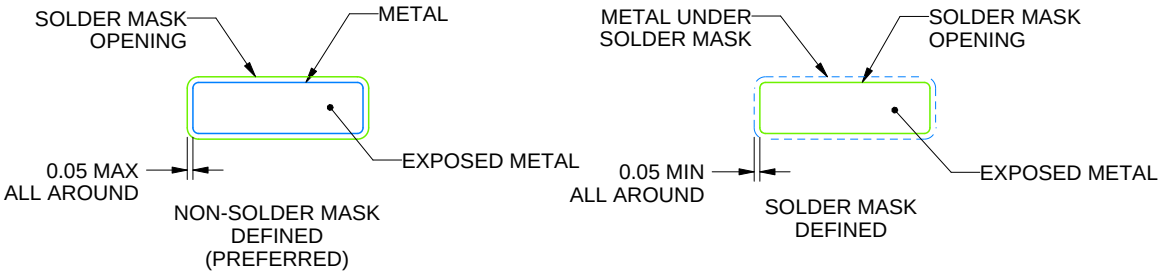
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE: 16X

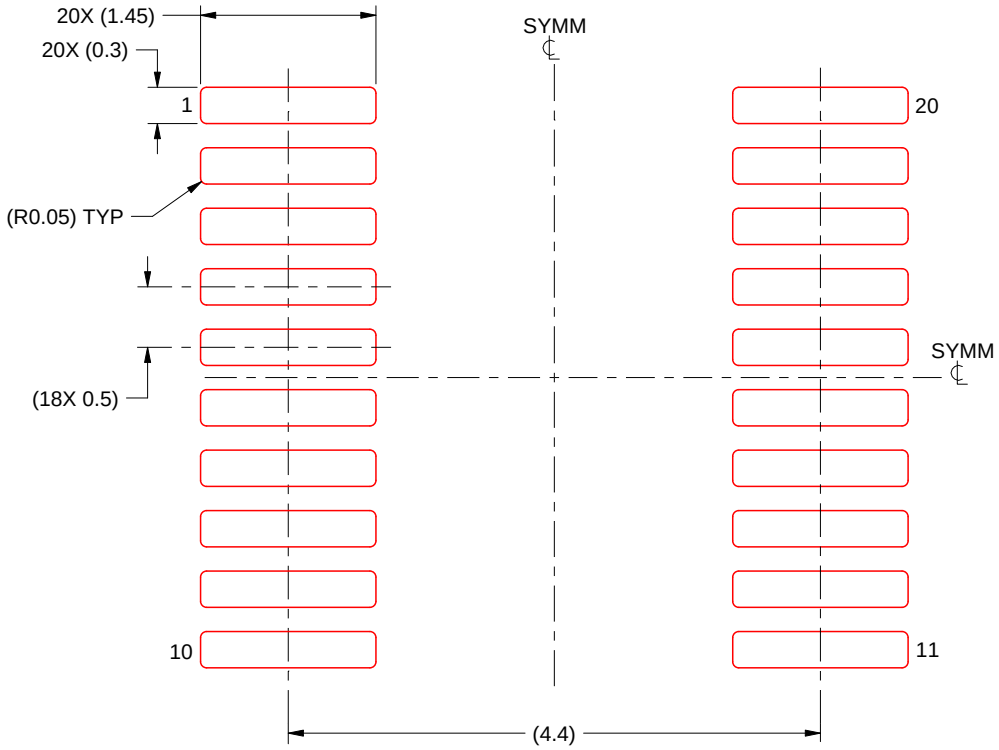


SOLDER MASK DETAILS

4226367/A 10/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226367/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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