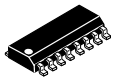
Presettable Divide-By-N Counter

MC14018B



SOIC-16
D SUFFIX
CASE 751B

The MC14018B contains five Johnson counter stages which are asynchronously presettable and resettable. The counters are synchronous, and increment on the positive going edge of the clock.

Presetting is accomplished by a logic 1 on the preset enable input. Data on the Jam inputs will then be transferred to their respective $\overline{Q}$ outputs (inverted). A logic 1 on the reset input will cause all $\overline{Q}$ outputs to go to a logic 1 state.

Division by any number from 2 to 10 can be accomplished by connecting appropriate $\overline{Q}$ outputs to the data input, as shown in the Function Selection table. Anti-lock gating is included in the MC14018B to assure proper counting sequence.

Features

- Fully Static Operation
- Schmitt Trigger on Clock Input
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4018B
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- This Device is Pb-Free and is RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

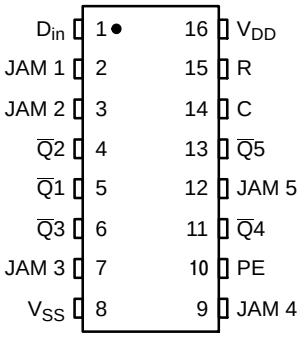
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: “D/DW” Packages: –7.0 mW/°C From 65 °C To 125 °C

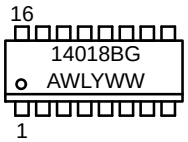
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



MARKING DIAGRAM



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb-Free Indicator

FUNCTIONAL TRUTH TABLE

Clock	Reset	Preset Enable	Jam Input	$\overline{Q}n$
↘	0	0	X	$\overline{Q}n$
↗	0	0	X	$\overline{D}_n$*
X	0	1	0	1
X	0	1	1	0
X	1	X	X	1

* D_n is the Data input for that stage. Stage 1 has Data brought out to Pin 1.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 2.

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55 °C Min	−55 °C Max	25 °C Min	25 °C Typ (Note 2)	25 °C Max	125 °C Min	125 °C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	– – –	0.05 0.05 0.05	– – –	0 0 0	0.05 0.05 0.05	– – –	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD} "1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	– – –	4.95 9.95 14.95	5.0 10 15	– – –	4.95 9.95 14.95	– – –	Vdc
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	– – –	1.5 3.0 4.0	– – –	2.25 4.50 6.75	1.5 3.0 4.0	– – –	1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) "1" Level (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	– – –	3.5 7.0 11	2.75 5.50 8.25	– – –	3.5 7.0 11	– – –	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	–3.0 –0.64 –1.6 –4.2	– – – –	–2.4 –0.51 –1.3 –3.4	–4.2 –0.88 –2.25 –8.8	– – – –	–1.7 –0.36 –0.9 –2.4	– – – –	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	– – –	0.51 1.3 3.4	0.88 2.25 8.8	– – –	0.36 0.9 2.4	– – –	mAdc
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	– – –	5.0 10 20	– – –	0.005 0.010 0.015	5.0 10 20	– – –	150 300 600	μAdc
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	I_T = (0.3 μA/kHz) f + I_{DD} I_T = (0.7 μA/kHz) f + I_{DD} I_T = (1.0 μA/kHz) f + I_{DD}							μAdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at 25 °C.
4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

ORDERING INFORMATION

Device	Package	Shipping†
MC14018BDG	SOIC-16 (Pb-Free)	48 Units / Rail
MC14018BDR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel

DISCONTINUED (Note 5)

NLV14018BDG*	SOIC-16 (Pb-Free)	48 Units / Rail

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

* NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

5. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

SWITCHING CHARACTERISTICS (Note 6) (C_L = 50 pF, T_A = 25 °C)

Characteristic	Symbol	V_{DD} Vdc	All Types Min	Typ (Note 7)	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 32 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.6 ns/pF) C_L + 20 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.4 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time Clock to $\overline{Q}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 265 ns		5.0	–	310	620	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 102 ns		10	–	120	240	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 72 ns		15	–	85	170	
Reset to $\overline{Q}$						ns
t_{PLH} = (0.90 ns/pF) C_L + 325 ns		5.0	–	370	740	
t_{PLH} = (0.36 ns/pF) C_L + 132 ns		10	–	150	300	
t_{PLH} = (0.26 ns/pF) C_L + 81 ns		15	–	100	200	
Preset Enable to $\overline{Q}$						ns
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 325 ns		5.0	–	370	740	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 132 ns		10	–	150	300	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 81 ns		15	–	100	200	
Setup Time Data (Pin 1) to Clock	t_{su}					ns
		5.0	200	0	–	
		10	100	0	–	
		15	80	0	–	
Jam Inputs to Preset Enable						ns
		5.0	200	0	–	
		10	100	0	–	
		15	80	0	–	
Data (Jam Inputs)−to−Preset Enable Hold Time	t_h	5.0	540	270	–	ns
		10	500	250	–	
		15	480	240	–	
Clock Pulse Width	t_{WH}	5.0	400	200	–	ns
		10	200	100	–	
		15	160	80	–	
Reset or Preset Enable Pulse Width	t_{WH}	5.0	290	145	–	ns
		10	130	65	–	
		15	110	55	–	
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0	No Limit			ns
		10				
		15				
Clock Pulse Frequency	f_{cl}	5.0	–	2.5	1.25	MHz
		10	–	6.5	3.25	
		15	–	8.0	4.0	

6. The formulas given are for the typical characteristics only at 25 °C.
7. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

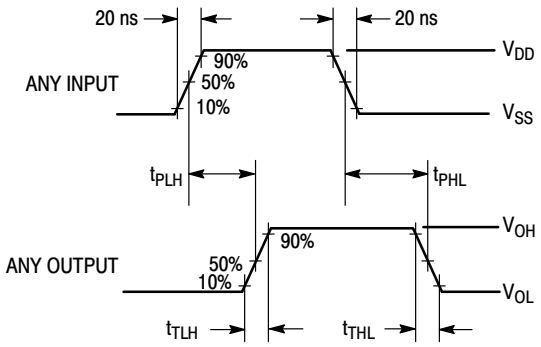
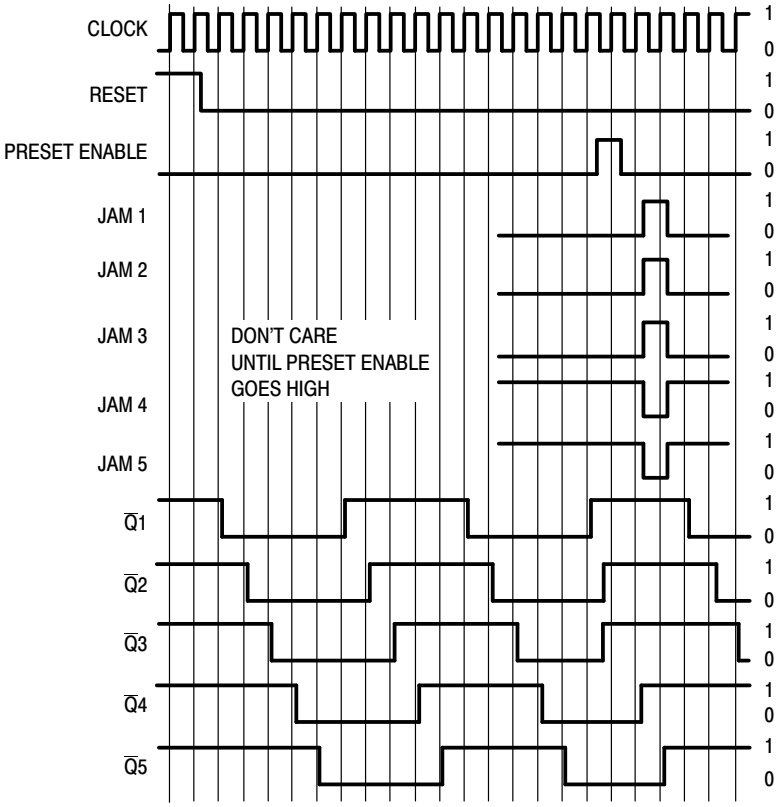


Figure 1. Switching Time Waveforms

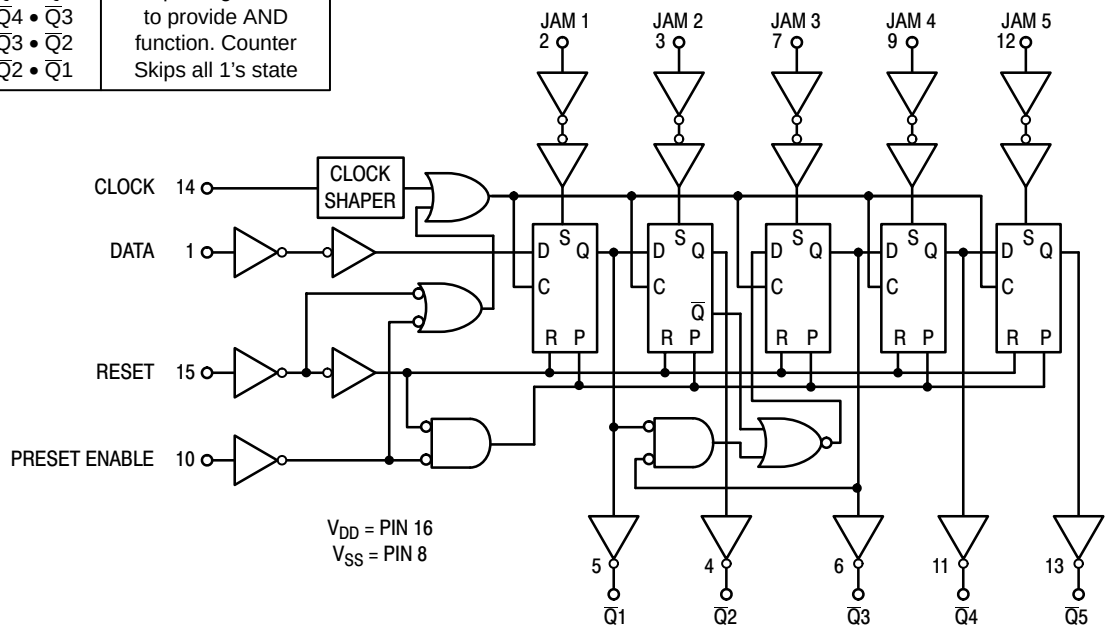
TIMING DIAGRAM
($\overline{Q}$5 Connected to Data Input)



FUNCTION SELECTION

Counter Mode	Connect Data Input (Pin 1) to:	Comments
Divide by 10 Divide by 8 Divide by 6 Divide by 4 Divide by 2	$\overline{Q}5$ $\overline{Q}4$ $\overline{Q}3$ $\overline{Q}2$ $\overline{Q}1$	No external components needed.
Divide by 9 Divide by 7 Divide by 5 Divide by 3	$\overline{Q}5 \bullet \overline{Q}4$ $\overline{Q}4 \bullet \overline{Q}3$ $\overline{Q}3 \bullet \overline{Q}2$ $\overline{Q}2 \bullet \overline{Q}1$	Gate package needed to provide AND function. Counter Skips all 1's state

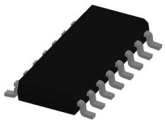
LOGIC DIAGRAM



REVISION HISTORY

Revision	Description of Changes	Date
9	Rebranded the Data Sheet to **onsemi** format. NLV14018BDG OPN Marked as Discontinued.	8/22/2025

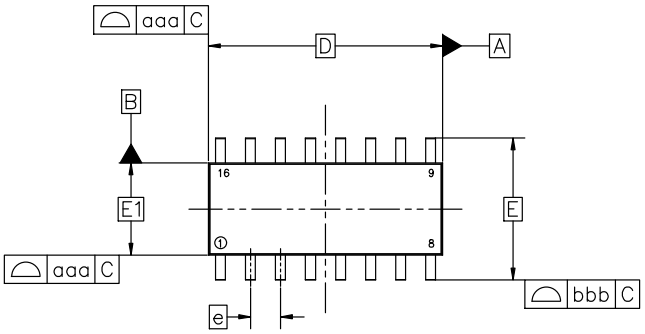
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



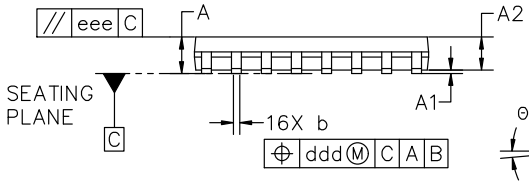
SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

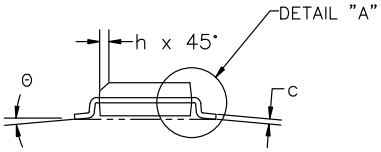
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



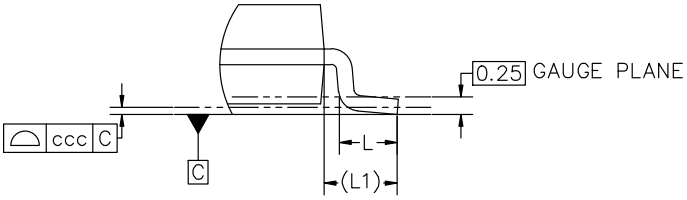
TOP VIEW



SIDE VIEW

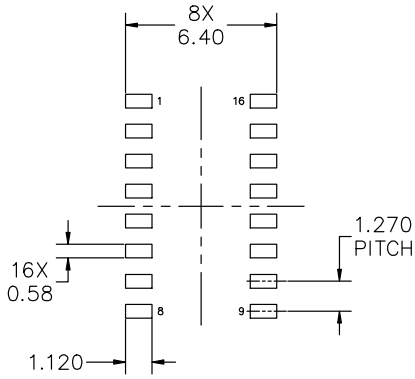


END VIEW



DETAIL "A"
Scale 3:1

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	---	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
Θ	0°	---	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

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DESCRIPTION:	SOIC−16 9.90X3.90X1.37 1.27P	PAGE 1 OF 2

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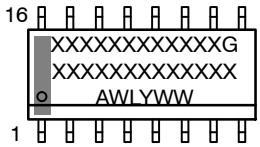
SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

PIN 1.	COLLECTOR
2.	BASE
3.	EMITTER
4.	NO CONNECTION
5.	EMITTER
6.	BASE
7.	COLLECTOR
8.	COLLECTOR
9.	BASE
10.	EMITTER
11.	NO CONNECTION
12.	EMITTER
13.	BASE
14.	COLLECTOR
15.	EMITTER
16.	COLLECTOR

STYLE 2:

PIN 1.	CATHODE
2.	ANODE
3.	NO CONNECTION
4.	CATHODE
5.	CATHODE
6.	NO CONNECTION
7.	ANODE
8.	CATHODE
9.	CATHODE
10.	ANODE
11.	NO CONNECTION
12.	CATHODE
13.	CATHODE
14.	NO CONNECTION
15.	ANODE
16.	CATHODE

STYLE 3:

PIN 1.	COLLECTOR, DYE #1
2.	BASE, #1
3.	EMITTER, #1
4.	COLLECTOR, #1
5.	COLLECTOR, #2
6.	BASE, #2
7.	EMITTER, #2
8.	COLLECTOR, #2
9.	COLLECTOR, #3
10.	BASE, #3
11.	EMITTER, #3
12.	COLLECTOR, #3
13.	COLLECTOR, #4
14.	BASE, #4
15.	EMITTER, #4
16.	COLLECTOR, #4

STYLE 4:

PIN 1.	COLLECTOR, DYE #1
2.	COLLECTOR, #1
3.	COLLECTOR, #2
4.	COLLECTOR, #2
5.	COLLECTOR, #3
6.	COLLECTOR, #3
7.	COLLECTOR, #4
8.	COLLECTOR, #4
9.	BASE, #4
10.	EMITTER, #4
11.	BASE, #3
12.	EMITTER, #3
13.	BASE, #2
14.	EMITTER, #2
15.	BASE, #1
16.	EMITTER, #1

STYLE 5:

PIN 1.	DRAIN, DYE #1
2.	DRAIN, #1
3.	DRAIN, #2
4.	DRAIN, #2
5.	DRAIN, #3
6.	DRAIN, #3
7.	DRAIN, #4
8.	DRAIN, #4
9.	GATE, #4
10.	SOURCE, #4
11.	GATE, #3
12.	SOURCE, #3
13.	GATE, #2
14.	SOURCE, #2
15.	GATE, #1
16.	SOURCE, #1

STYLE 6:

PIN 1.	CATHODE
2.	CATHODE
3.	CATHODE
4.	CATHODE
5.	CATHODE
6.	CATHODE
7.	CATHODE
8.	CATHODE
9.	ANODE
10.	ANODE
11.	ANODE
12.	ANODE
13.	ANODE
14.	ANODE
15.	ANODE
16.	ANODE

STYLE 7:

PIN 1.	SOURCE N-CH
2.	COMMON DRAIN (OUTPUT)
3.	COMMON DRAIN (OUTPUT)
4.	GATE P-CH
5.	COMMON DRAIN (OUTPUT)
6.	COMMON DRAIN (OUTPUT)
7.	COMMON DRAIN (OUTPUT)
8.	SOURCE P-CH
9.	SOURCE P-CH
10.	COMMON DRAIN (OUTPUT)
11.	COMMON DRAIN (OUTPUT)
12.	COMMON DRAIN (OUTPUT)
13.	GATE N-CH
14.	COMMON DRAIN (OUTPUT)
15.	COMMON DRAIN (OUTPUT)
16.	SOURCE N-CH

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