Fixed Frequency, 99% Duty Cycle Peak Current Mode Notebook System Power Controller

Check for Samples: TPS51220

FEATURES

- **Input Voltage Range: 4.5 V to 28 V**
- **Output Voltage Range: 1 V to 12 V**
- **Selectable Light Load Operation (Continuous / Auto Skip / Out-Of-Audio™ Skip)**
- **Programmable Droop Compensation**
- **Voltage Servo Adjustable Soft Start**
- **200 kHz to 1 MHz Fixed Frequency PWM**
- **Selectable Current/ D-CAP™ Mode Architecture**
- **180° Phase Shift Between Channels**
- **Resistor or Inductor DCR Current Sensing**
- **Powergood Output for Each Channel**
- **OCL/OVP/UVP/UVLO Protections (OVP Disable Option)**
- **Thermal Shutdown (Non-Latch)**
- **Output Discharge Function (Disable Option)**
- **Integrated Boot Strap MOSFET Switch**
- **QFN-32 (RHB)**

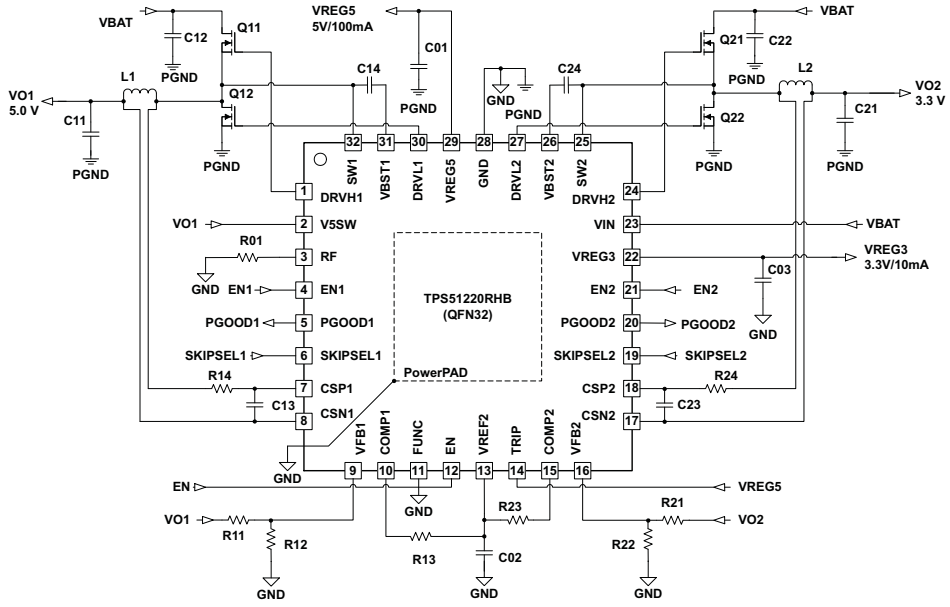
APPLICATIONS

- **Notebook Computer System and I/O Bus**
- **Point of Load in LCD TV, MFP**

DESCRIPTION

The TPS51220 is a dual synchronous buck regulator controller with 2 LDOs. It is optimized for 5-V/3.3-V system controller, enabling designers to cost effectively complete 2-cell to 4-cell notebook system power supply. The TPS51220 supports high efficiency, fast transient response and 99% duty cycle operation. It supports supply input voltage ranging from 4.5 V to 28 V, and output voltages from 1 V to 12 V. Two types of control schemes can be chosen depending on the application. Peak current mode supports stability operation with lower ESR capacitor and output accuracy. The D-CAP mode supports fast transient response. The high duty (99%) operation and the wide input/output voltage range supports flexible design for small mobile PCs and a wide variety of other applications. The fixed frequency can be adjusted from 200 kHz to 1 MHz by a resistor, and each channel runs 180° out of phase. The TPS51220 can also synchronize to the external clock, and the interleaving ratio can be adjusted by its duty. The TPS51220 is available in the 32 pin 5x5 QFN package and is specified from –40°C to 85°C.

Figure 1. TYPICAL APPLICATION CIRCUIT



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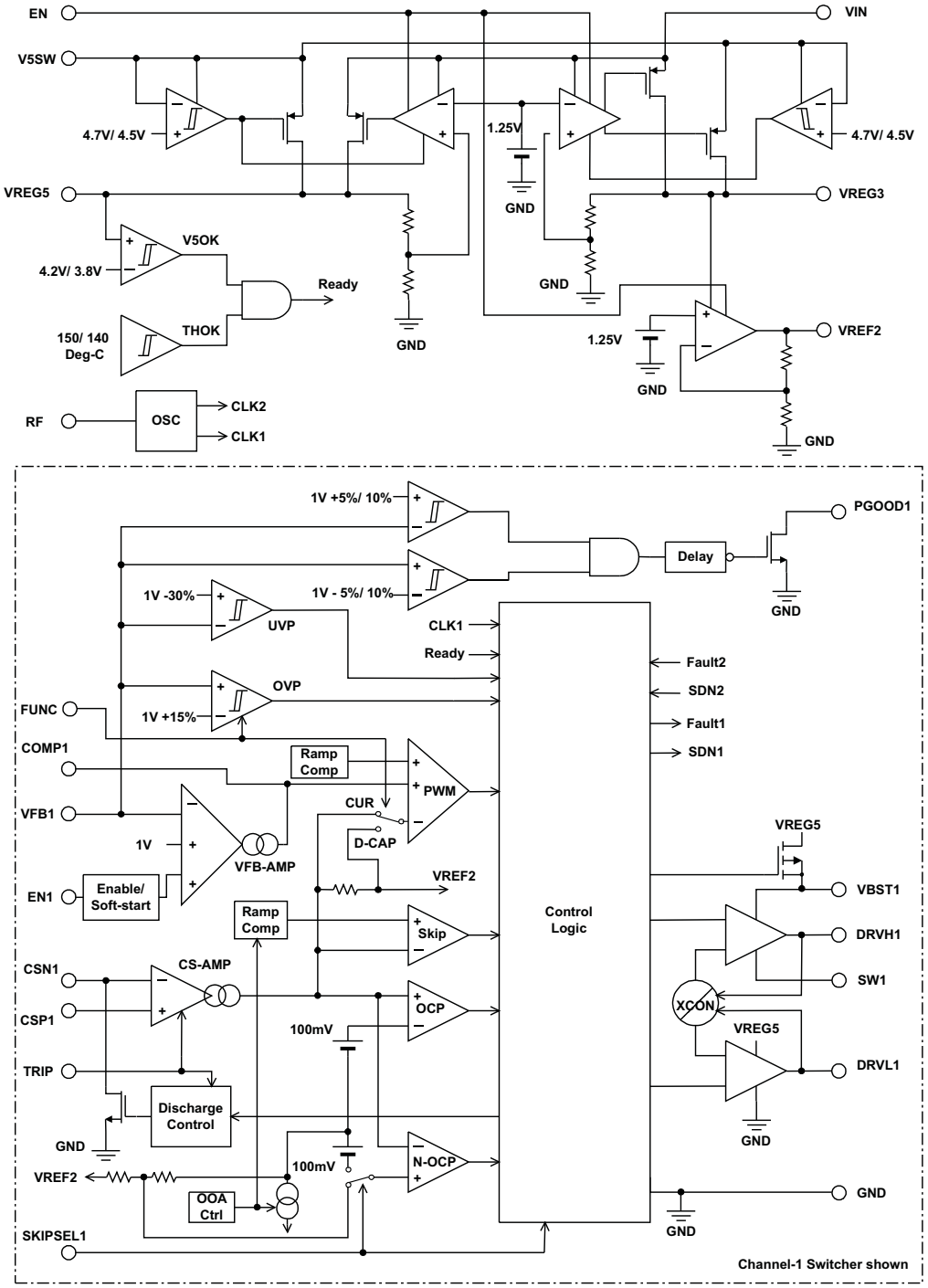
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
V_I	Input voltage range (2)	VIN	–0.3 to 30	V
		VBST1, VBST2	–0.3 to 35	V
		VBST1, VBST2(3)	–0.3 to 7	V
		SW1, SW2	–7 to 30	V
		CSP1, CSP2, CSN1, CSN2	–1 to 13.5	V
		EN, EN1, EN2, VFB1, VFB2, TRIP, SKIPSEL1, SKIPSEL2, FUNC	–0.3 to 7	V
		V5SW	–0.3 to 7	V
		V5SW (to VREG5)(4)	–7 to 7	V
V_O	Output voltage range(2)	DRVH1, DRVH2	–7 to 35	V
		DRVH1, DRVH2 (3)	–0.3 to 7	V
		DRVL1, DRVL2, COMP1, COMP2, VREG5, RF, VREF2, PGOOD1, PGOOD2	–0.3 to 7	V
		VREG3	–0.3 to 3.6	V
T_J	Operating junction temperature range		–40 to 125	°C
T_{stg}	Storage temperature		–55 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.
(3) Voltage values are with respect to the corresponding SW terminal.
(4) When EN is high and V5SW is grounded, or voltage is applied to V5SW when EN is low.

DISSIPATION RATINGS (2 oz. Trace and Copper Pad with Solder)

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
32 pin RHB	2.2 W	23 mW/°C	0.9 W

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
V_{SS}	Supply voltage	VIN	4.5		28	V
		V5SW	–0.8		6	
V_I V_O	I/O voltage	DRVH1, DRVH2	–4.0		33	V
		VBST1, VBST2,	–0.1		33	
		DRVH1, DRVH2 (wrt SW1, SW2)	–0.1		6	
		DRVH1, DRVH2 (negative overshoot -6 V for t< 20% duration of switching period)	–6		33	
		SW1, SW2	–4.0		28	
		SW1, SW2 (negative overshoot -6 V for t< 20% duration of switching period)	–6		28	
		CSP1, CSP2, CSN1, CSN2	–0.8		13	
		EN, EN1, EN2, VFB1, VFB2, TRIP, DRVL1, DRVL2, COMP1, COMP2, VREG5, RF, VREF2, PGOOD1, PGOOD2, SKIPSEL1, SKIPSEL2, FUNC	–0.1		6	
		VREG3	–0.1		3.5	
T_A	Operating free-air temperature		–40		85	°C

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ORDERING INFORMATION

T_A	PACKAGE(1)	ORDERABLE PART NUMBER	TRANSPORT MEDIA	QUANTITY
-40°C to 85°C	Plastic Quad Flat Pack (32 Pin QFN)	TPS51220RHBT	Tape and Reel	250
		TPS51220RHBR	Tape and Reel	3000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

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ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, EN = 3.3V, VIN = 12V, V5SW = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
$I_{(VINSDN)}$	VIN shutdown current	VIN shutdown current, T_A = 25°C, No Load, EN = 0V, V5SW = 0 V			7	15	µA
$I_{(VINSTBY)}$	VIN standby current	VIN standby current, T_A = 25°C, No Load, EN1 = EN2 = V5SW = 0 V			80	120	µA
$I_{(VBATSTBY)}$	V_{BAT} standby current	V_{BAT} standby current, T_A = 25°C, No Load SKIPSEL2 = 2V, EN2 = open, EN1 = V5SW = 0V(1)			500		µA
$I_{(V5SW)}$	V5SW supply current	V5SW current, T_A = 25°C, No Load, ENx = 5V, VFBx = 1.05 V	TRIP = 5 V		1.2		mA
			TRIP = 0 V		1.4		mA
VREF2 OUTPUT							
$V_{(VREF2)}$	VREF2 output voltage	$I_{(VREF2)}$ < ±10 µA, T_A = 25°C		1.98	2.00	2.02	V
		$I_{(VREF2)}$ < ±100 µA, 4.5V < VIN < 25 V		1.97	2.00	2.03	
VREG3 OUTPUT							
$V_{(VREG3)}$	VREG3 output voltage	V5SW = 0 V, $I_{(VREG3)}$ = 0 mA, T_A = 25°C		3.279	3.313	3.347	V
		V5SW = 0 V, 0 mA < $I_{(VREG3)}$ < 10 mA, 5.5 V < VIN < 25 V		3.135	3.300	3.400	
$I_{(VREG3)}$	VREG3 output current	VREG3 = 3 V		10	15	20	mA
VREG5 OUTPUT							
$V_{(VREG5)}$	VREG5 output voltage	V5SW = 0 V, $I_{(VREG5)}$ = 0 mA, T_A = 25°C		4.99	5.04	5.09	V
		V5SW = 0 V, 0 mA < $I_{(VREG5)}$ < 100 mA, 6 V < VIN < 25 V		4.90	5.03	5.15	
		V5SW = 0 V, 0 mA < $I_{(VREG5)}$ < 100 mA, 5.5 V < VIN < 25 V		4.50	5.03	5.15	V
$I_{(VREG5)}$	VREG5 output current	V5SW = 0 V, VREG5 = 4.5 V		100	150	200	mA
		V5SW = 5 V, VREG5 = 4.5 V		200	300	400	
$V_{(THV5SW)}$	Switchover threshold	Turning on		4.55	4.7	4.8	V
		Hysteresis		0.15	0.20	0.25	
$t_{d(V5SW)}$	Switchover delay	Turning on			7.7		ms
$R_{(V5SW)}$	5V SW on-resistance	$I_{(VREG5)}$ = 100 mA			0.5		Ω
OUTPUT							
$V_{(VFB)}$	$V_{F\ B}$ regulation voltage tolerance	T_A = 25°C, No Load		0.9925	1.000	1.0075	V
		T_A = –40°C to 85°C , No Load		0.990	1.000	1.010	
$I_{(VFB)}$	$V_{F\ B}$ input current	VFBx = 1.05 V, COMPx = 1.8 V, T_A = 25°C		–50		50	nA
$R_{(Dischg)}$	CSNx discharge resistance	ENx = 0 V, CSNx = 0.5 V, T_A = 25°C			20	40	Ω
VOLTAGE TRANSCONDUCTANCE AMPLIFIER							
Gmv	Gain	T_A = 25°C			500		µS
V_{ID}	Differential input voltage range			–30		30	mV
$I_{(COMPSINK)}$	COMP maximum sink current	COMPx = 1.8 V			33		µA
$I_{(COMPSRC)}$	COMP maximum source current	COMPx = 1.8 V			–33		µA

(1) Specified by design. Detail external condition follows application circuit of Figure 53.

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ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, EN = 3.3V, VIN = 12V, V5SW = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT AMPLIFIER						
G_C	Gain	TRIP = 0V/2V, CSN = 5V, T_A = 25°C (2)		3.333		
		TRIP = 3.3V/5V, CSN = 5V, T_A = 25°C (2)		1.667		
V_{IC}	Common mode input voltage range		0		13	V
V_{ID}	Differential input voltage range	T_A = 25°C	–75		75	mV
POWERGOOD						
$V_{(THPG)}$	PG threshold	PG in from lower	92.5%	95%	97.5%	
		PG in from higher	102.5%	105%	107.5%	
		PG hysteresis		5%		
$I_{(PG)}$	PG sink current	PGOOD = 0.5 V		5		mA
$t_{(PGDLY)}$	PGOOD delay	Delay for PG in	0.8	1	1.2	ms
SOFTSTART						
$t_{(SSDYL)}$	Soft-start delay time	Delay for Soft Start, ENx = Hi to SS-ramp starts		200		µs
$t_{(SS)}$	Soft-start Time	Internal Soft Start		960		µs
FREQUENCY AND DUTY CONTROL						
$f_{(SW)}$	Switching frequency	Rf = 330 kΩ	273	303	333	kHz
$V_{(THRF)}$	RF threshold	Lo to Hi	0.7	1.3	2	V
		Hysteresis		0.2		V
$f_{(SYNC)}$	Syncronization Input Frequency Range (2)		200		1000	kHz
t_{ON}min	Minimum On Time	$V_{(DRVH)}$ = 90% to 10%, No Load		120	150	ns
t_{OFF}min	Minimum Off Time	$V_{(DRVH)}$ = 10% to 90%, No Load		290	440	ns
t_D	Dead time	DRVH-off to DRVL-on	10	30	50	ns
		DRVL-off to DRVH-on	30	40	70	ns
$V_{(DTH)}$	DRVH-off threshold	DRVH to GND (2)		1		V
$V_{(DTL)}$	DRVL-off threshold	DRVL to GND (2)		1		V
OUTPUT DRIVERS						
$R_{(DRVH)}$	DRVH resistance	Source, $V_{(VBST-DRVH)}$ = 0.1 V		1.7	5	Ω
		Sink, $V_{(DRVH-SW)}$ = 0.1 V		1	3	
$R_{(DRVL)}$	DRVL resistance	Source, $V_{(VREG5-DRVL)}$ = 0.1 V		1.3	4	Ω
		Sink, $V_{(DRVL-GND)}$ = 0.1 V		0.7	2	
CURRENT SENSE						
$V_{(OCL-ULV)}$	Current limit threshold (ultra-low voltage)	TRIP = 0V/2V, T_A = 25°C	27	31	35	mV
		TRIP = 0V/2V	25	31	37	
$V_{(OCL-LV)}$	Current limit threshold (low voltage)	TRIP = 3.3V/5V, T_A = 25°C	56	60	64	
		TRIP = 3.3V/5V	54	60	66	
$V_{(ZC)}$	Zero cross detection comparator Offset	0.95V < CSNx < 12.6V	–4	0	4	mV
$V_{(OCLN-ULV)}$	Negative current limit threshold (ultra-low voltage)	TRIP = 0V/2V, T_A = 25°C	–24	–31	–38	mV
		TRIP = 0V/2V	–22	–31	–40	
$V_{(OCLN-LV)}$	Negative current limit threshold (low voltage)	TRIP = 3.3V/5V, T_A = 25°C	–51	–60	–69	
		TRIP = 3.3V/5V	–49	–60	–71	

(2) Specified by design.

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ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, EN = 3.3V, VIN = 12V, V5SW = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UVP, OVP AND UVLO						
$V_{(OVP)}$	OVP Trip Threshold	OVP detect	110%	115%	120%	
$t_{(OVPDLY)}$	OVP Prop Delay			1.5		µs
$V_{(UVP)}$	UVP Trip Threshold	UVP detect	65%	70%	73%	
$t_{(UVPDLY)}$	UVP Delay		0.8	1	1.2	ms
$V_{(UVREF2)}$	VREF2 UVLO Threshold	Wake up	1.7	1.8	1.9	V
		Hysteresis	75	100	125	mV
$V_{(UVREG3)}$	VREG3 UVLO Threshold	Wake up	3	3.1	3.2	V
		Hysteresis	0.10	0.15	0.20	
$V_{(UVREG5)}$	VREG5 UVLO Threshold	Wake up	4.1	4.2	4.3	V
		Hysteresis	0.35	0.40	0.44	V
INTERFACE AND LOGIC THRESHOLD						
$V_{(EN)}$	EN Threshold	Wake up	0.8	1	1.2	V
		Hysteresis	0.1	0.2	0.3	
$V_{(EN12)}$	EN1/EN2 Threshold	Wake up	0.45	0.50	0.55	V
		Hysteresis	0.1	0.2	0.3	
$V_{(EN12SS)}$	EN1/EN2 SS Start Threshold	SS-ramp start threshold at external soft start		1		V
$V_{(EN12SSEND)}$	EN1/EN2 SS End Threshold	SS-End threshold at external soft start (3)		2		V
$I_{(EN12)}$	EN1/EN2 Source Current	VEN1/EN2 = 0V	1.5	2	2.6	µA
$V_{(SKIPSEL)}$	SKIPSEL1/SKIPSEL2 Setting Voltage	Continuous			1.5	V
		Auto Skip	1.9		2.1	
		OOA Skip (min 1/8 Fsw)	3.2		3.4	
		OOA Skip (min 1/16 Fsw)	3.8			
$V_{(TRIP)}$	TRIP Setting Voltage	$V_{(OCL-ULV)}$, Discharge ON			1.5	V
		$V_{(OCL-ULV)}$, Discharge OFF	1.9		2.1	
		$V_{(OCL-LV)}$, Discharge OFF	3.2		3.4	
		$V_{(OCL-LV)}$, Discharge ON	3.8			
$V_{(FUNC)}$	FUNC Setting Voltage	Current mode, OVP enable			1.5	V
		D-CAP mode, OVP disable	1.9		2.1	
		D-CAP mode, OVP enable	3.2		3.4	
		Current mode, OVP disable	3.8			
$I_{(TRIP)}$	TRIP Input Current	TRIP = 0 V	–1		1	µA
		TRIP =5 V	–1		1	
$I_{(SKIPSEL)}$	SKIPSEL Input Current	SKIPSELx = 0 V	–0.5		0.5	µA
		SKIPSELx = 5 V	–0.5		0.5	
BOOT STRAP SW						
$V_{(FBST)}$	Forward Voltage	$V_{VREG5-VBST}$, I_F = 10 mA, T_A = 25°C		0.10	0.20	V
$I_{(BSTLK)}$	VBST Leakage Current	VBST = 30 V, SW = 25 V		0.01	1.5	µA
THERMAL SHUTDOWN						
$T_{(SDN)}$	Thermal SDN Threshold	Shutdown temperature (3)		150		°C
		Hysteresis (3)		10		

(3) Specified by design.

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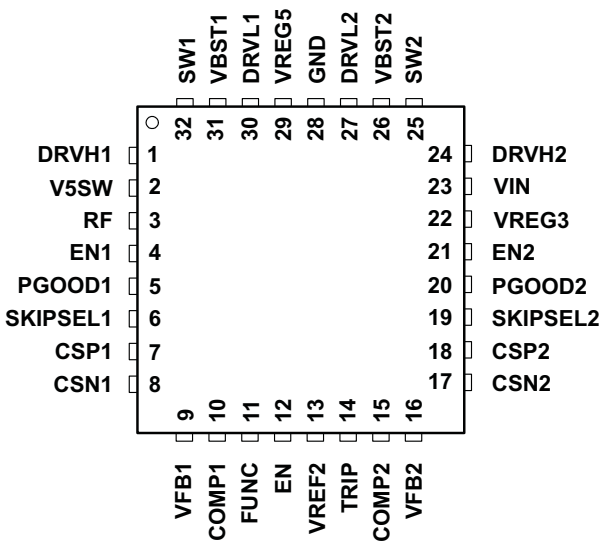
DEVICE INFORMATION

PINOUT

RHB PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
DRVH1	1	O	High-side MOSFET gate driver outputs. Source 1.7Ω, sink 1.0Ω, SW-node referenced floating driver. Drive voltage corresponds to VBST to SW voltage.
DRVH2	24		
SW2	25	I/O	High-side MOSFET gate driver returns.
SW1	32		
VREG3	22	O	Always alive 3.3-V, 10-mA low dropout linear regulator output. Bypass to (signal) GND with more than 1-μF ceramic capacitor. Runs from VIN supply or from VREG5 when it is switched over to V5SW input.
EN1	4	I	Channel 1 and channel 2 SMPS enable Pins. When turning on, apply greater than 0.55 V and less than 6 V, or be floating. Connect to GND to disable. Adjustable soft-start capacitance to be attached here.
EN2	21		
PGOOD1	5	O	Power Good window comparator outputs for channel 1 and channel 2. The applied voltage should be less than 6 V, and the recommended pull-up resistance value is from 100 kΩ to 1 MΩ.
PGOOD2	20		
SKIPSEL1	6	I	Skip mode selection pin. GND: Continuous conduction mode VREF2: Auto skip VREG3: OOA auto skip, maximum 7 skips (suitable for f_{sw} < 400 kHz) VREG5: OOA auto skip, maximum 15 skips (suitable for equal to or greater than 400 kHz)
SKIPSEL2	19		
CSP1	7	I/O	Current sense comparator inputs (+). An RC network with high quality X5R or X7R ceramic capacitor should be used to extract voltage drop across DCR. 0.1 μF is a good value to start the design. See the current sensing scheme section for more details.
CSP2	18		
CSN1	8	I	Current sense comparator inputs (–). See the current sensing scheme section. Used as power supply for the current sense circuit for 5 V or higher output voltage setting. Also, used for output discharge terminal.
CSN2	17		
VFB1	9	I	SMPS voltage feedback inputs. Connect the feedback resistors divider, and should be referred to (signal) GND.
VFB2	16		
COMP1	10	I	Loop compensation pin for current mode (error amplifier output). Connect R (and C if required) from this pin to VREF2 for proper loop compensation with current mode operation. Ramp compensation adjustable pin for D-CAP mode, connect R from this pin to VREF2. 10 kΩ is a good value to start the design. 6 kΩ to 20 kΩ can be chosen. See the D-CAP MODE section for more details.
COMP2	15		
RF	3	I/O	Frequency setting pin. Connect a frequency setting resistor to (signal) GND. Connect to an external clock for synchronization.

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TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
FUNC	11	I	Control architecture and OVP function selection pin. GND: Current mode, OVP enable VREF2: D-CAP mode, OVP disable VREG3: D-CAP mode, OVP enable VREG5: Current mode, OVP disable
VREF2	13	O	2-V Reference Output. Bypass to (signal) GND by 0.22µF ceramic capacitor.
TRIP	14	I	Overcurrent trip level and discharge mode selection pin. GND: $V_{(OCL-ULV)}$, Discharge on VREF2: $V_{(OCL-ULV)}$, Discharge off VREG3: $V_{(OCL-LV)}$, Discharge off VREG5: $V_{(OCL-LV)}$, Discharge on
EN	12	I	VREF2 and VREG5 Linear Regulators Enable Pin. When turning on, apply greater than 1.2V and less than 6V. Connect to GND to Disable.
VBST1	31	I	Supply inputs for high-side NFET driver (boot strap Terminal). Connect a capacitor (0.1µF or greater is recommended) from this pin to respective SW terminal. Additional SB diode from VREG5 to this pin is an optional.
VBST2	26		
DRVL1	30	O	Low-side MOSFET gate driver outputs. Source 1.3 Ω, sink 0.7 Ω, GND referenced driver.
DRVL2	27		
V5SW	2	I	VREG5 switchover power supply input pin. When EN1 is high, PGOOD1 indicates *GOOD* and V5SW voltage is higher than 4.8 V, switch-over function will be enabled. (Note) When switch-over is enabled, VREG5 output voltage will be almost the same as V5SW input voltage.
VREG5	29	O	5-V, 100-mA low-dropout linear regulator output. Bypass to (power) GND using a 10-µF ceramic capacitor. Runs from VIN supply. Internally connected to VBST and DRVL. Shuts off with EN. Switches over to V5SW when 4.8 V or above is provided. (Note: when switch-over (above V5SW) is enabled, VREG5 output voltage is approximately the same as V5SW input voltage.)
VIN	23	I	Supply input for 5-V and 3.3-V linear regulator. Typically connected to VBAT.
GND	28	–	Ground.

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TYPICAL CHARACTERISTICS

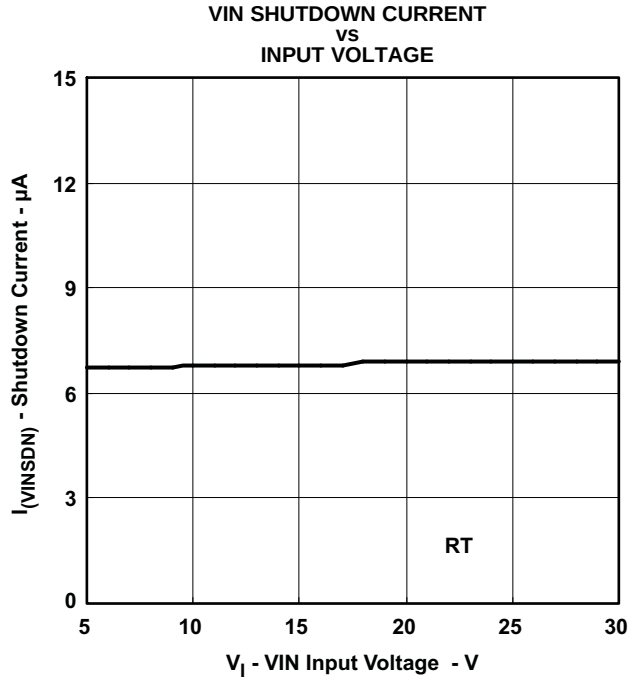

Figure 2.

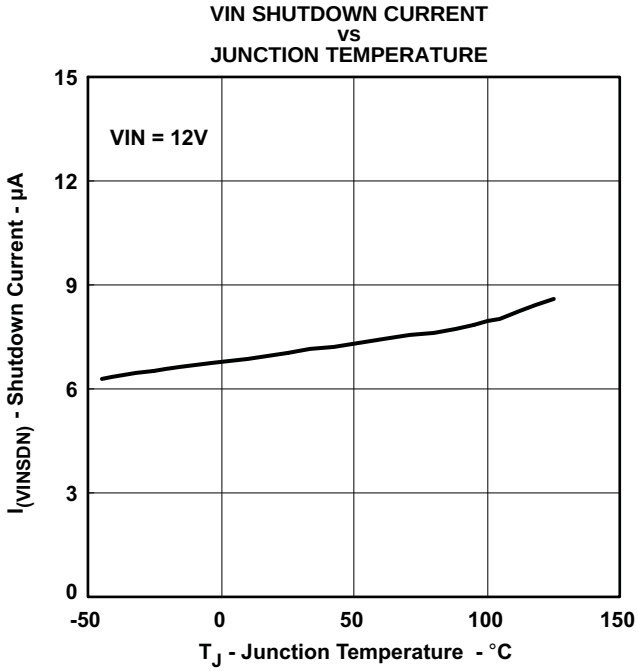

Figure 3.

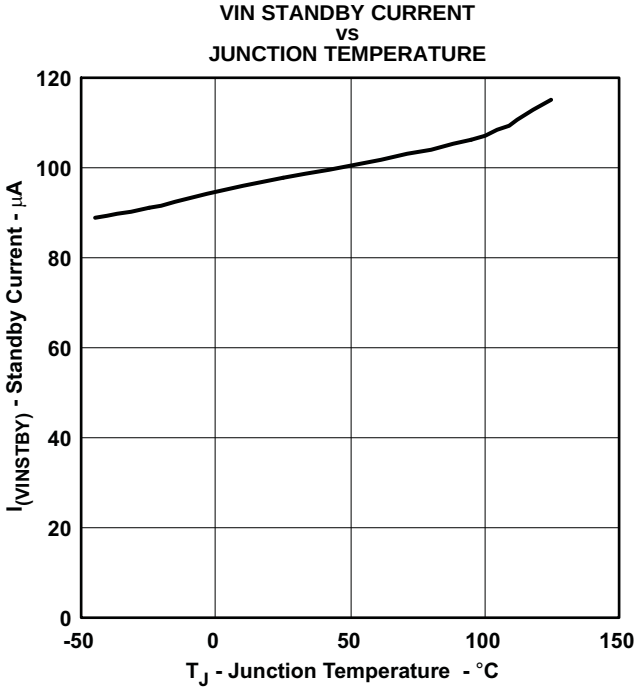

Figure 4.

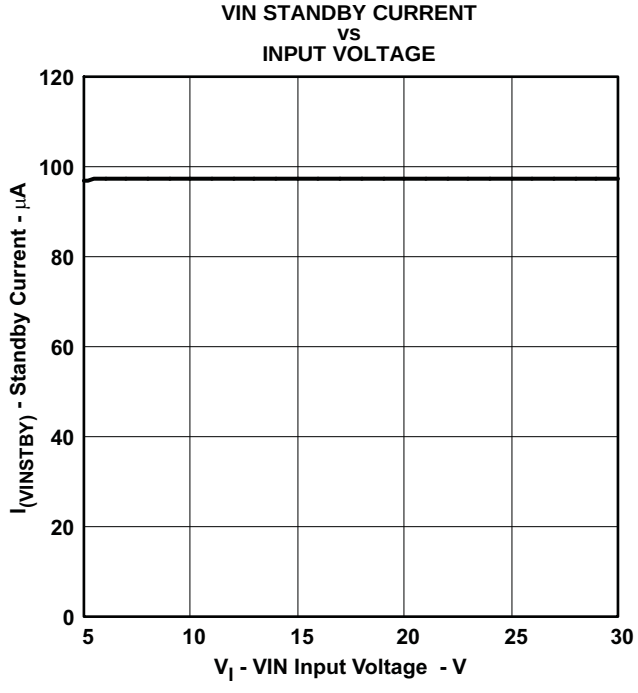

Figure 5.

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TYPICAL CHARACTERISTICS (continued)

NO LOAD BATTERY CURRENT
vs
INPUT VOLTAGE

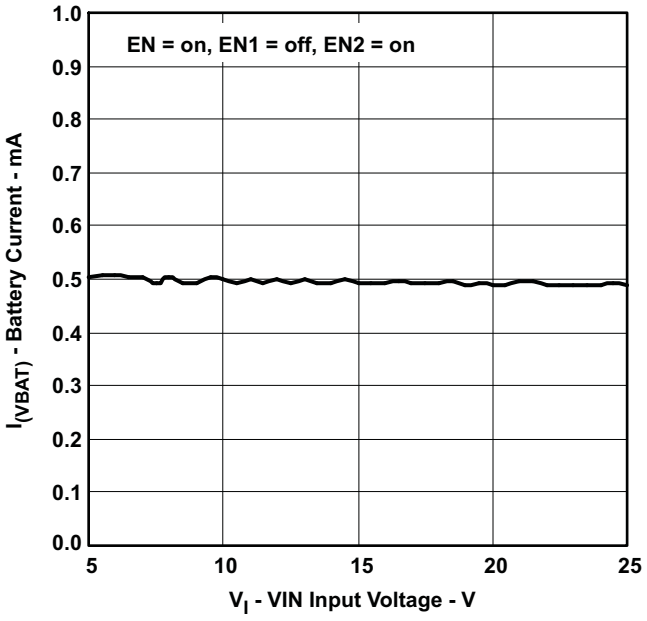

Figure 6.

NO LOAD BATTERY CURRENT
vs
INPUT VOLTAGE

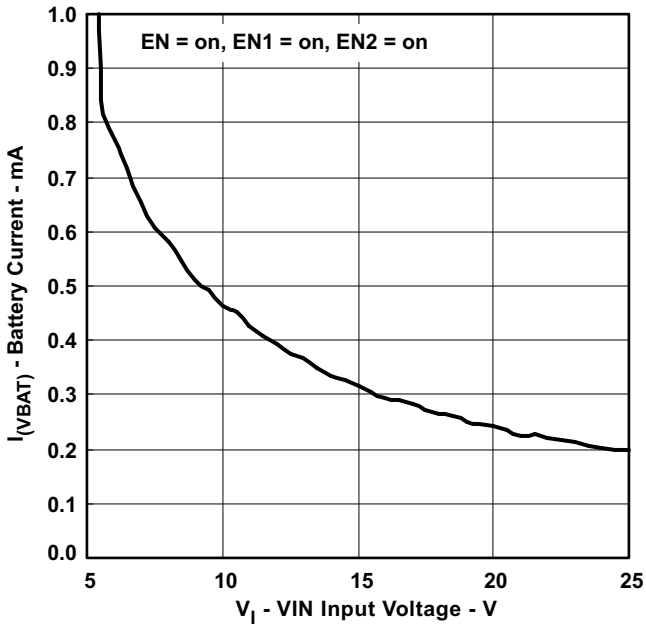

Figure 7.

BATTERY CURRENT
vs
INPUT VOLTAGE

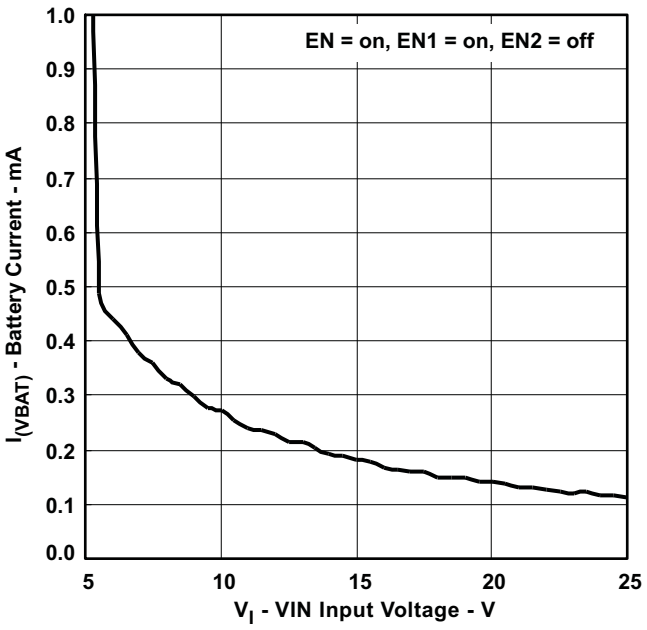

Figure 8.

VREF2 OUTPUT VOLTAGE
vs
OUTPUT CURRENT

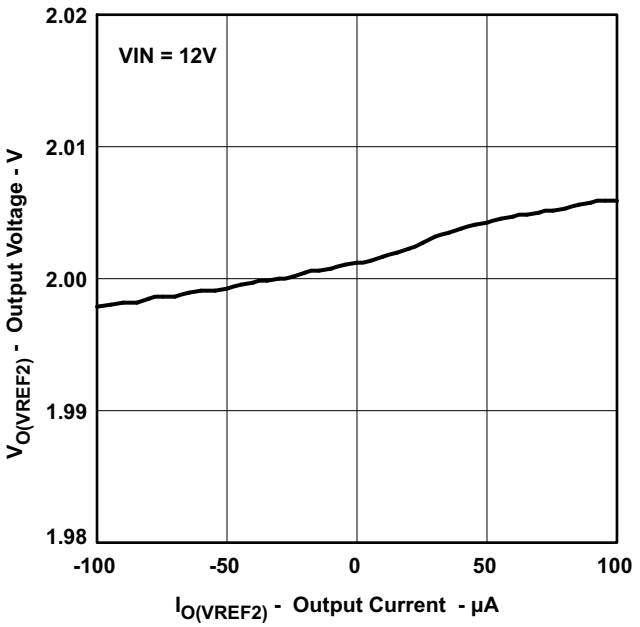

Figure 9.

TYPICAL CHARACTERISTICS (continued)

VREG3 OUTPUT VOLTAGE
vs
OUTPUT CURRENT

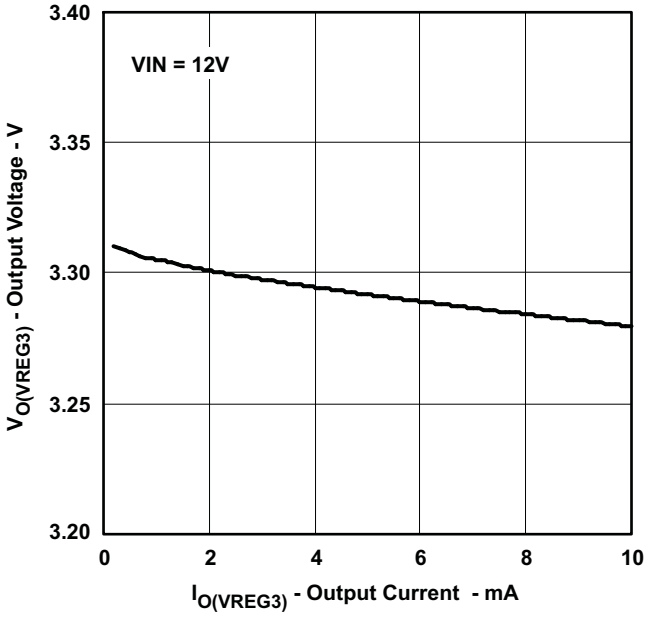

Figure 10.

VREG5 OUTPUT VOLTAGE
vs
OUTPUT CURRENT

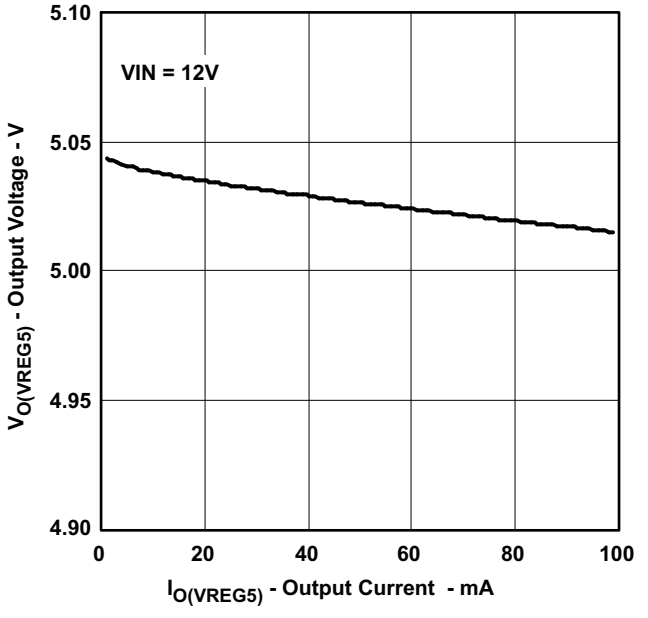

Figure 11.

SWITCHING FREQUENCY
vs
JUNCTION TEMPERATURE

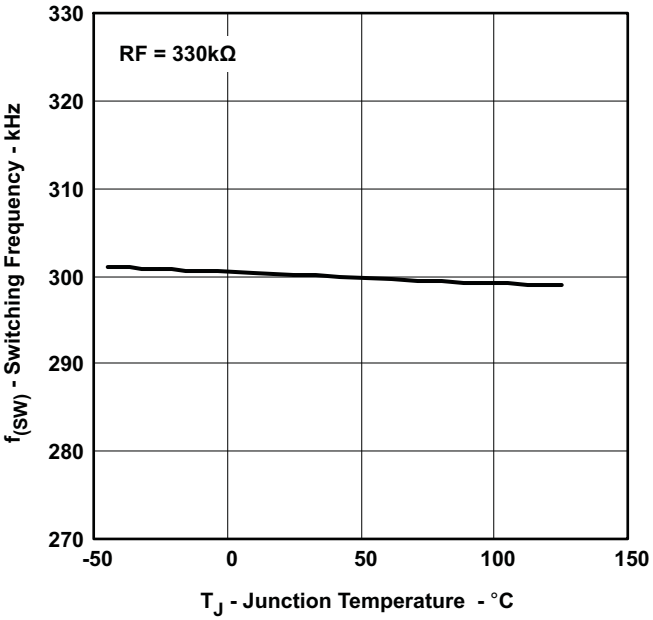

Figure 12.

FORWARD VOLTAGE OF BOOST SW
vs
JUNCTION TEMPERATURE

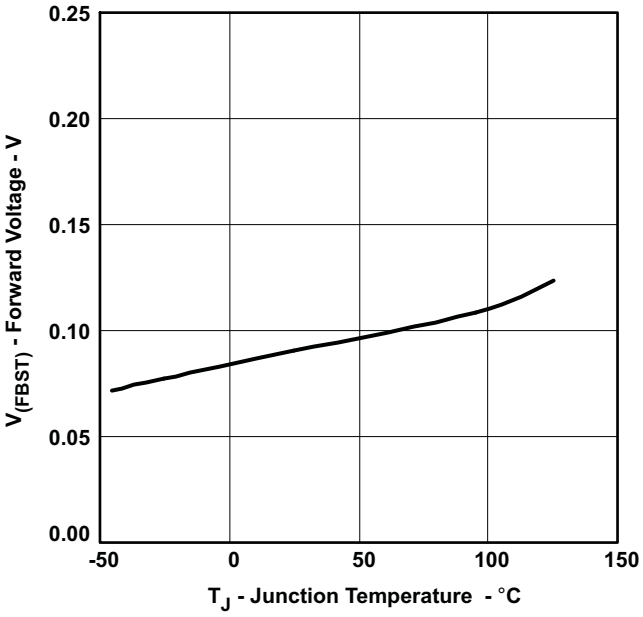

Figure 13.

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TYPICAL CHARACTERISTICS (continued)

OVP/UVP THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

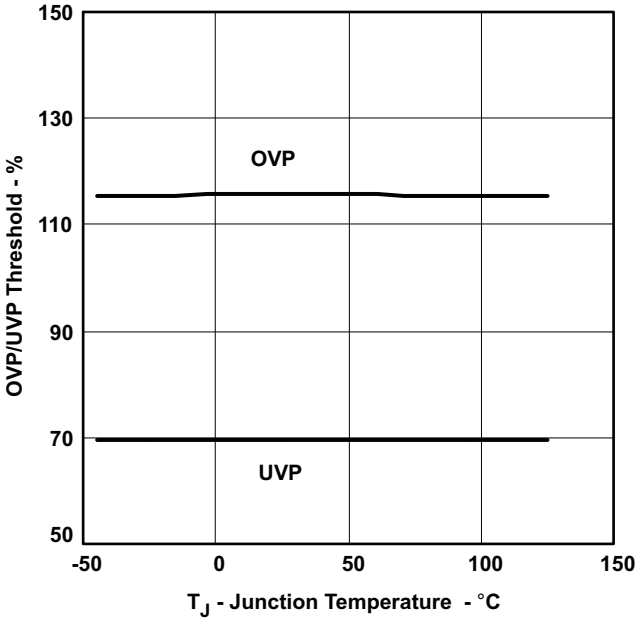

Figure 14.

VBST LEAKAGE CURRENT
vs
JUNCTION TEMPERATURE

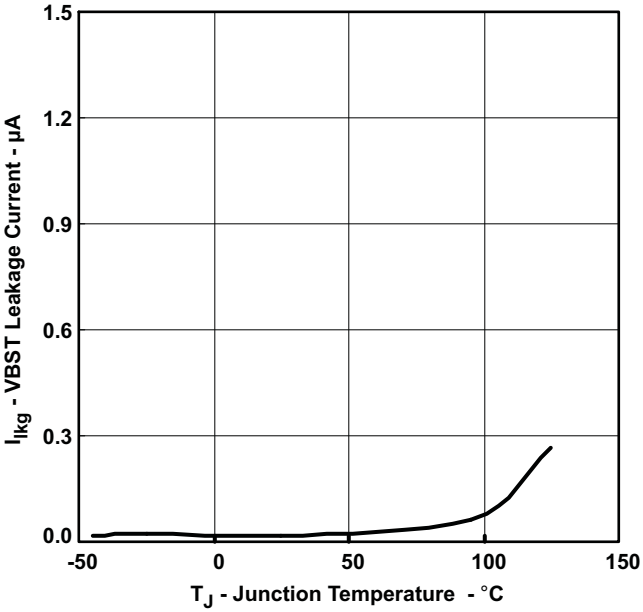

Figure 15.

CURRENT LIMIT THRESHOLD
vs
JUNCTION TEMPERATURE

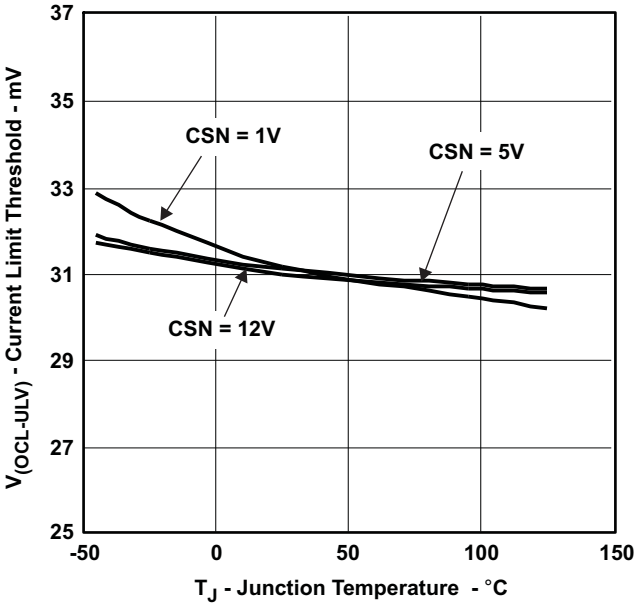

Figure 16.

CURRENT LIMIT THRESHOLD
vs
JUNCTION TEMPERATURE

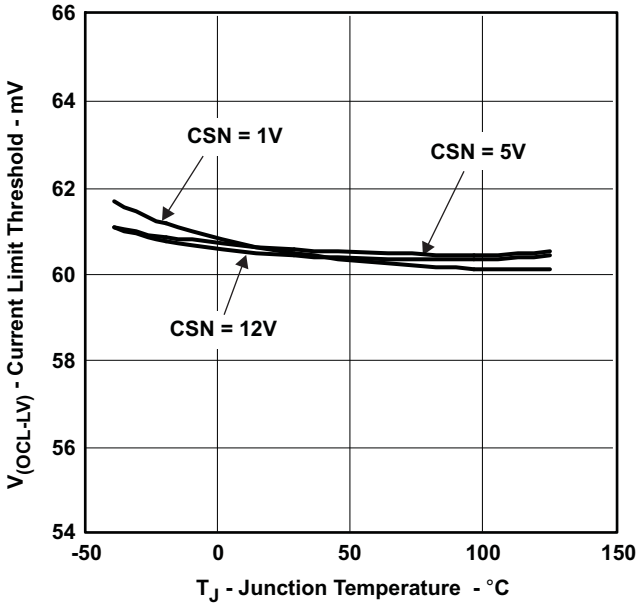

Figure 17.

TYPICAL CHARACTERISTICS (continued)

5-V OUTPUT VOLTAGE
vs
INPUT VOLTAGE

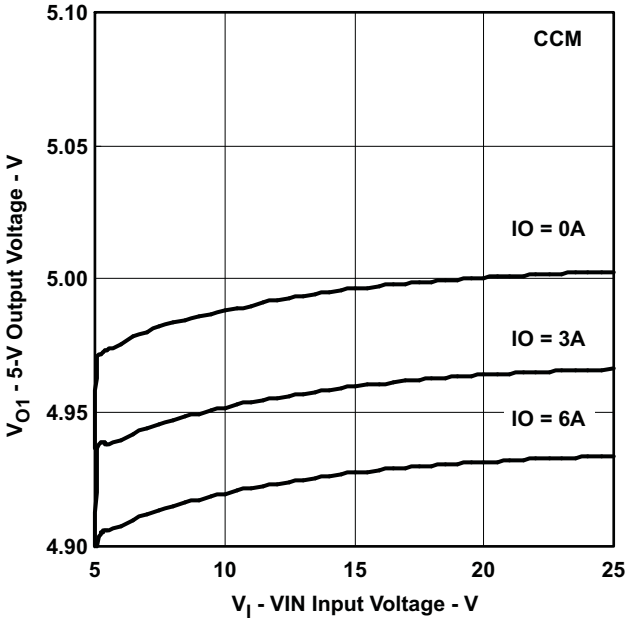

Figure 18.

3.3-V OUTPUT VOLTAGE
vs
INPUT VOLTAGE

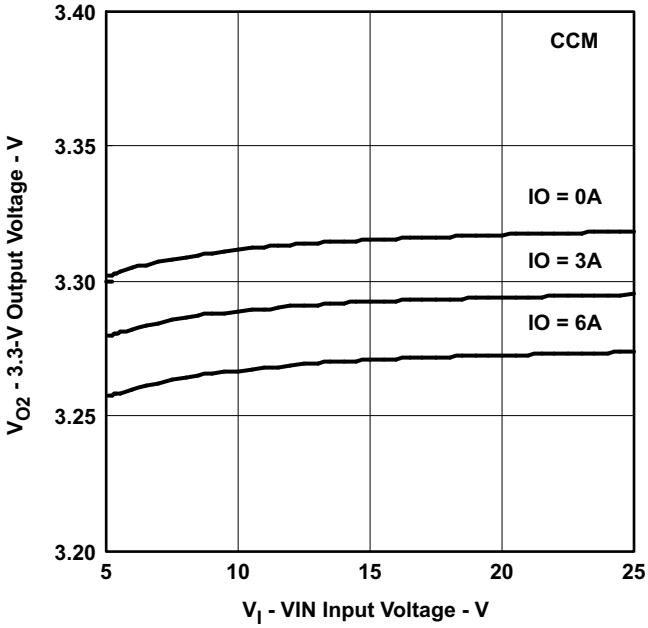

Figure 19.

5-V EFFICIENCY
vs
OUTPUT CURRENT

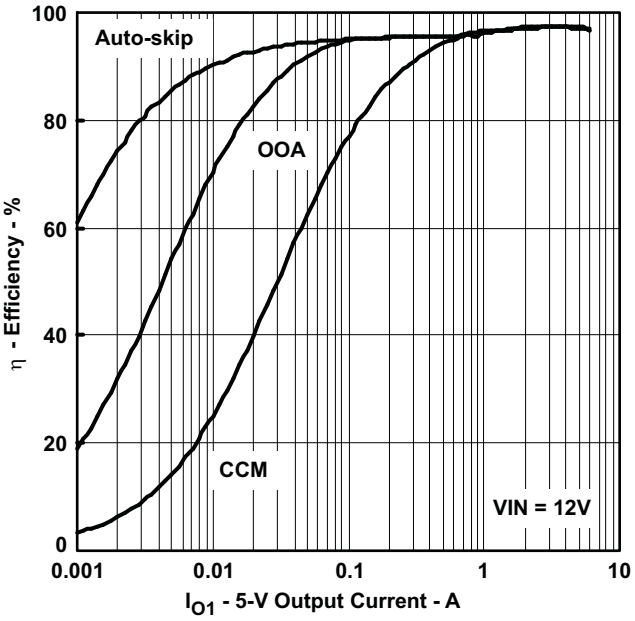

Figure 20.

5-V EFFICIENCY
vs
OUTPUT CURRENT

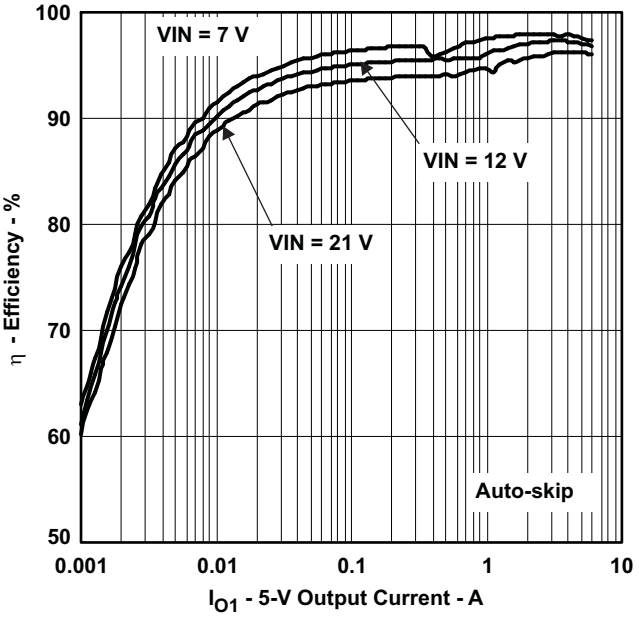

Figure 21.

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TYPICAL CHARACTERISTICS (continued)

3.3-V EFFICIENCY vs OUTPUT CURRENT

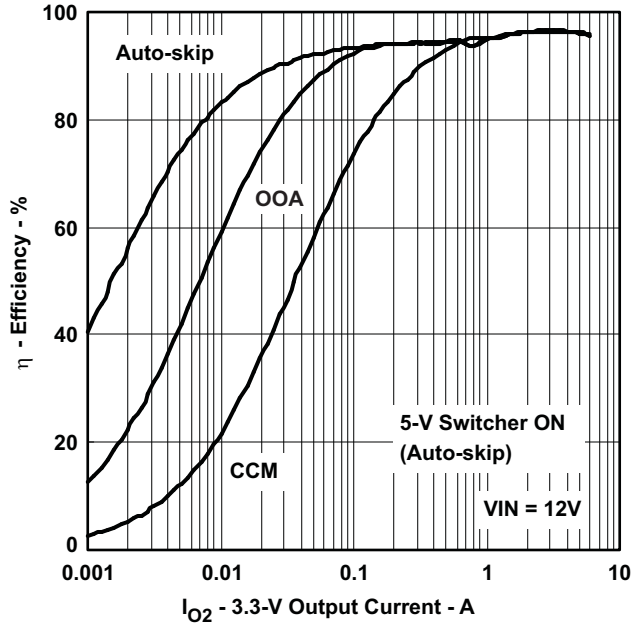

Figure 22.

3.3-V EFFICIENCY vs OUTPUT CURRENT

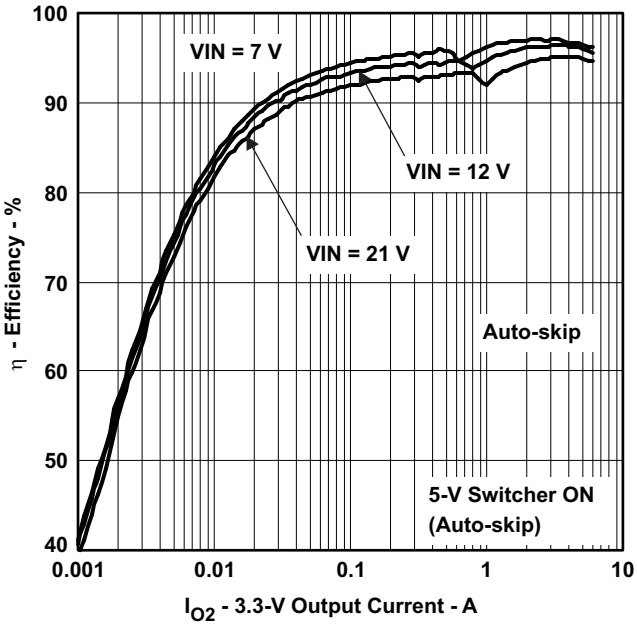

Figure 23.

5-V SWITCHING FREQUENCY vs OUTPUT CURRENT

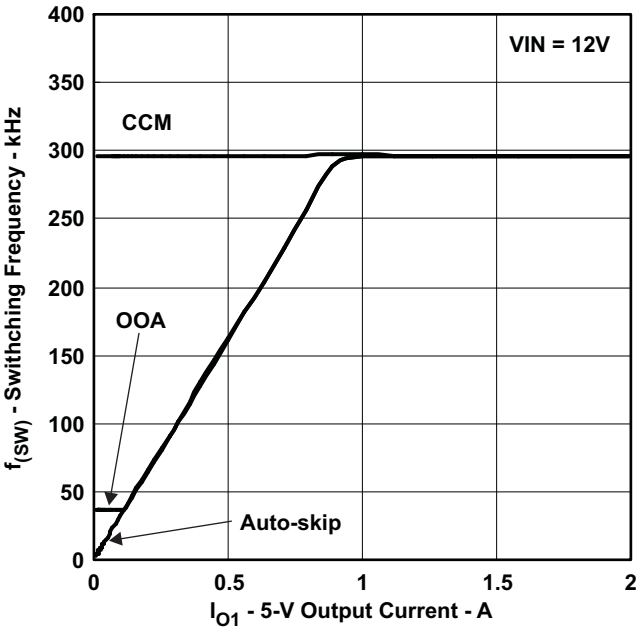

Figure 24.

3.3-V SWITCHING FREQUENCY vs OUTPUT CURRENT

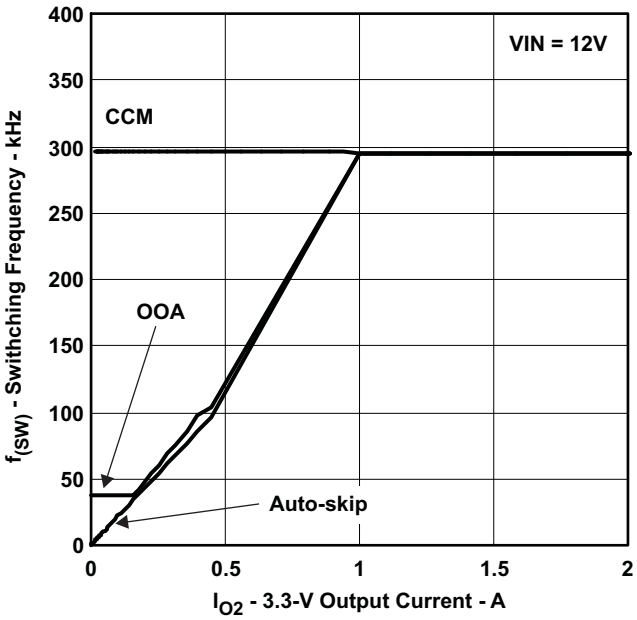

Figure 25.

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TYPICAL CHARACTERISTICS (continued)

5-V OUTPUT VOLTAGE
vs
OUTPUT CURRENT

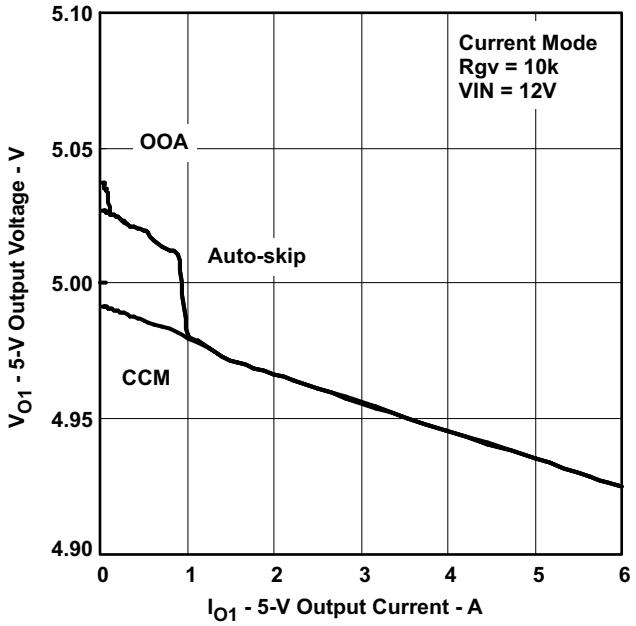

Figure 26.

3.3-V OUTPUT VOLTAGE
vs
OUTPUT CURRENT

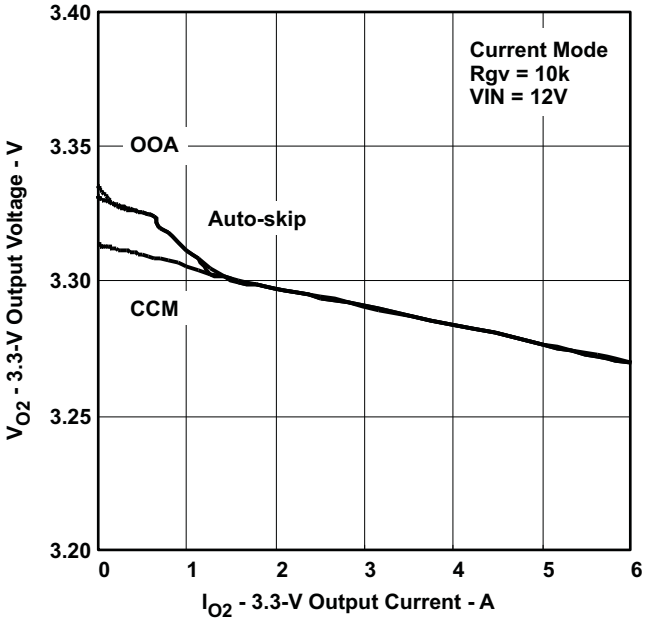

Figure 27.

5-V OUTPUT VOLTAGE
vs
OUTPUT CURRENT

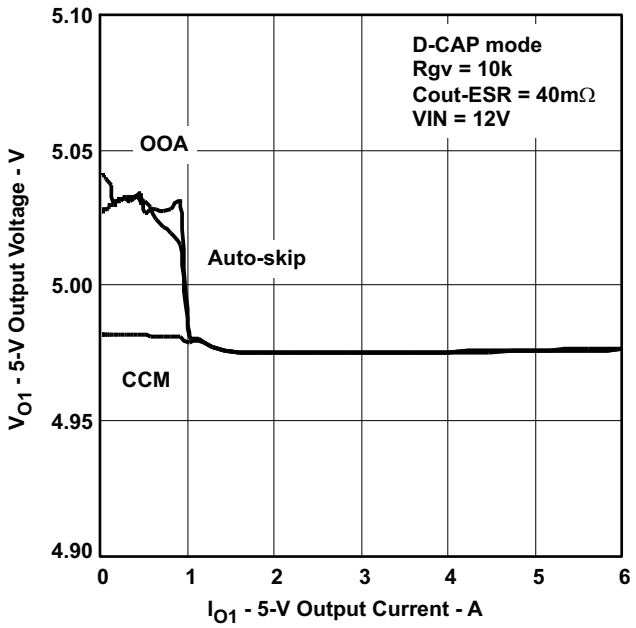

Figure 28.

3.3-V OUTPUT VOLTAGE
vs
OUTPUT CURRENT

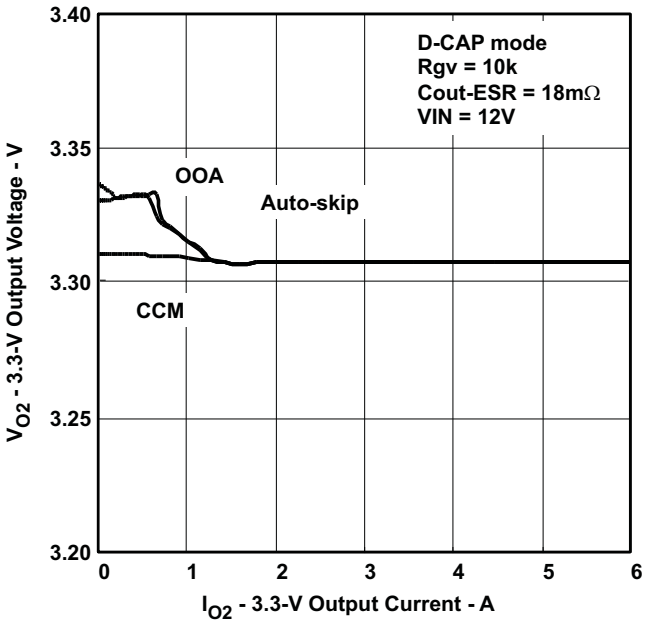

Figure 29.

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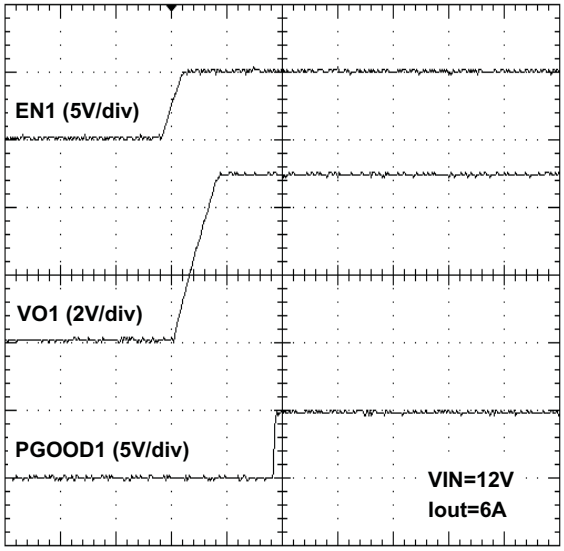
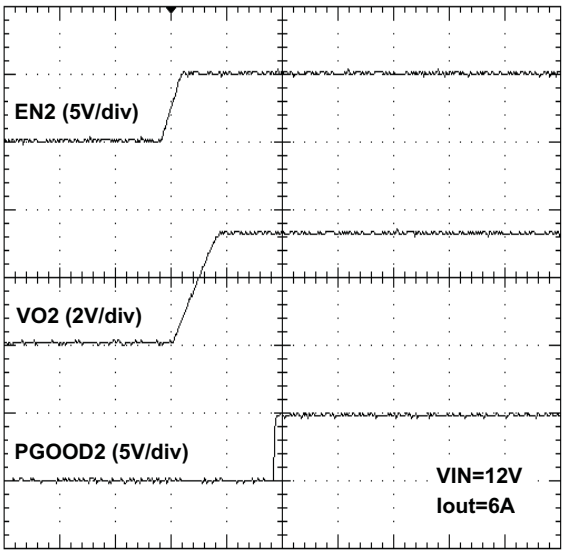
TYPICAL CHARACTERISTICS (continued)

5.0-V START-UP WAVEFORMS



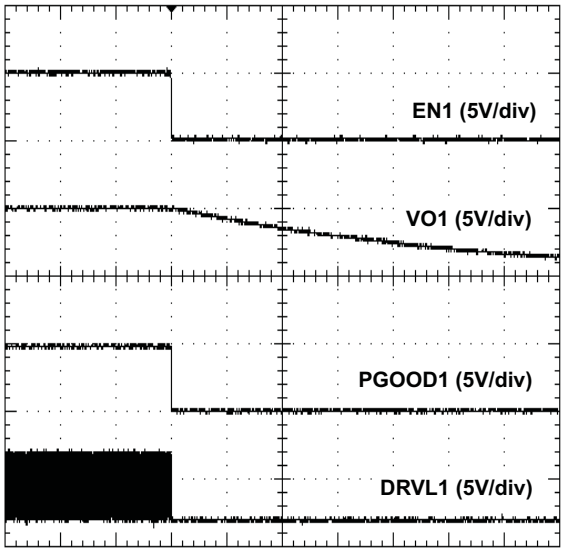
t - Time - 1ms/div
Figure 30.

3.3-V START-UP WAVEFORMS



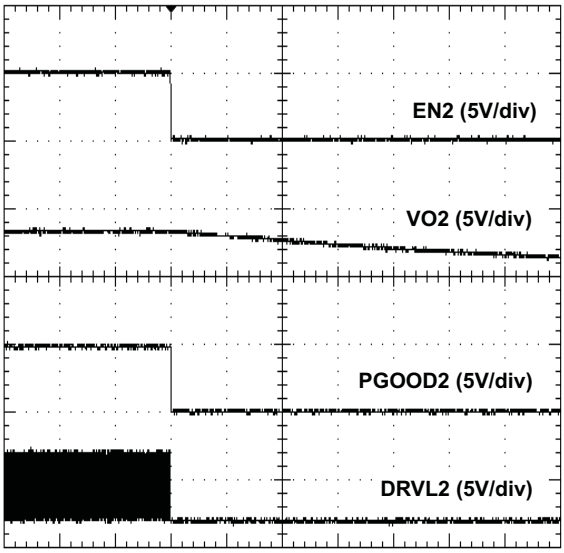
t - Time - 1ms/div
Figure 31.

5.0-V SOFT-STOP WAVEFORMS



t - Time - 1ms/div
Figure 32.

3.3-V SOFT-STOP WAVEFORMS



t - Time - 1ms/div
Figure 33.

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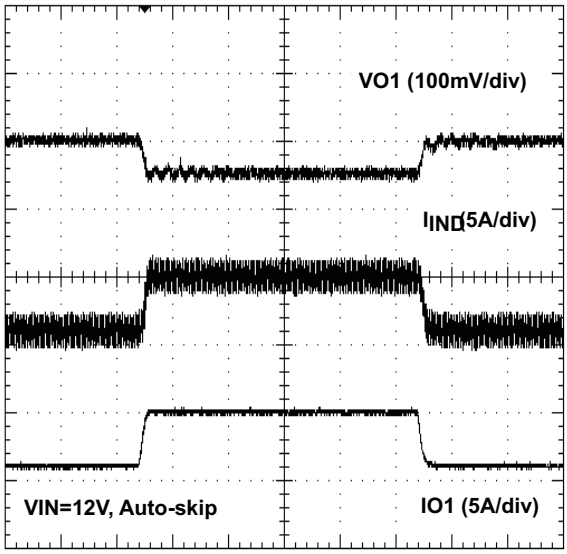
TYPICAL CHARACTERISTICS (continued)

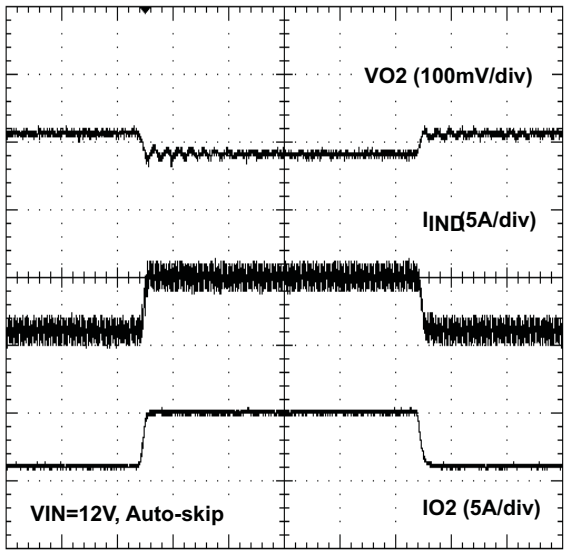
5.0-V LOAD TRANSIENT RESPONSE



t - Time - 100 μs/div

Figure 34.

3.3-V LOAD TRANSIENT RESPONSE



t - Time - 100 μs/div

Figure 35.

5.0-V BODE-PLOT – GAIN AND PHASE vs FREQUENCY

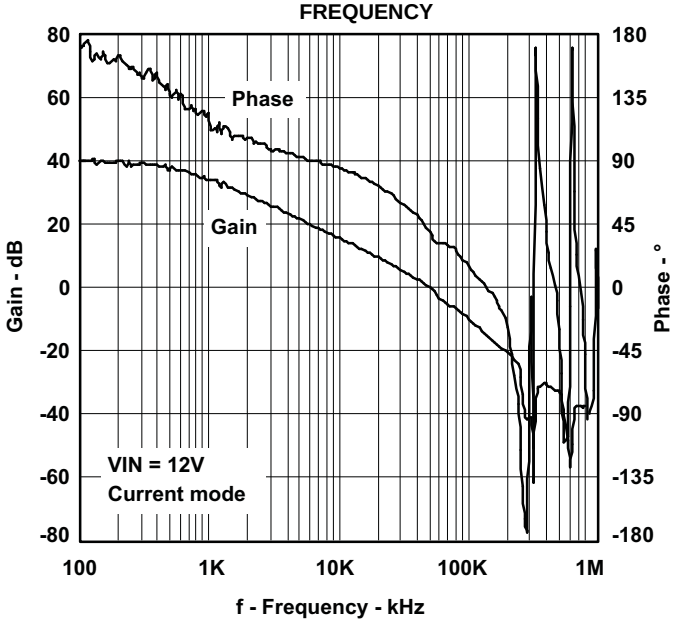


Figure 36.

3.3-V BODE-PLOT – GAIN AND PHASE vs FREQUENCY

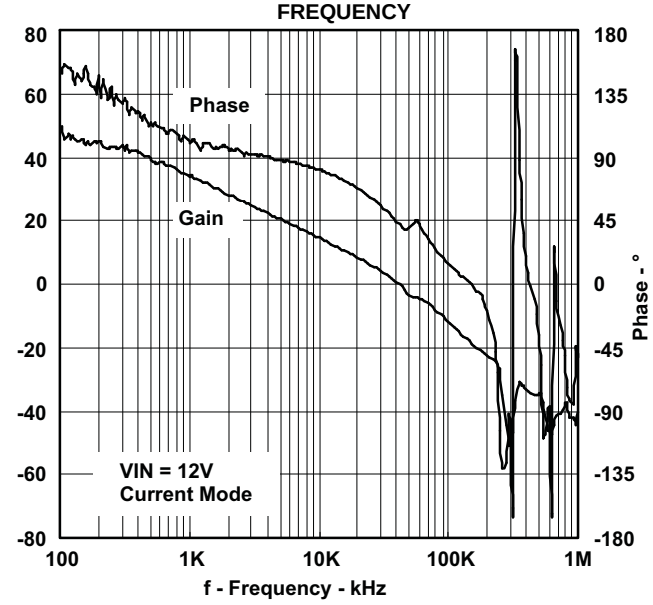


Figure 37.

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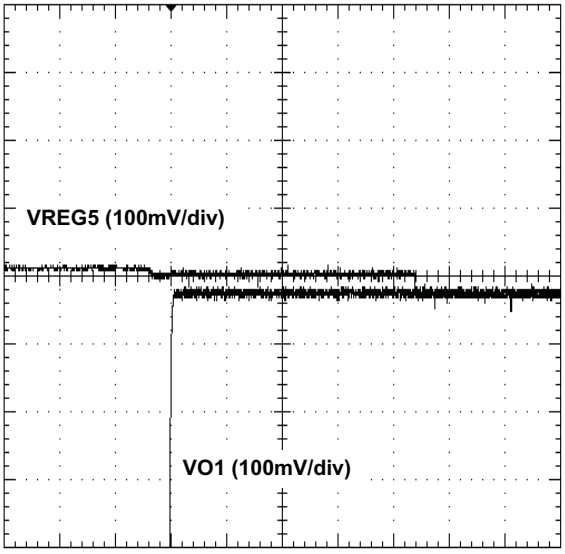
TYPICAL CHARACTERISTICS (continued)

5.0-V SWITCH-OVER WAVEFORMS



t - Time - 2ms/div
Figure 38.

DETAILED DESCRIPTION

ENABLE AND SOFT START

When EN is *Low*, the TPS51220 is in the shutdown state. The 3.3-V LDO only stays alive, and consumes 7 µA (typically). When EN becomes *High*, the TPS51220 is in the standby state. The 2-V reference and the 5-V LDO become enabled, and consume approximately 80 µA with no load condition, and are ready to turn on SMPS channels. Each SMPS channel is turned on when ENx becomes *High*. After ENx is set to high, the TPS51220 begins softstart, and ramps up the output voltage from zero to the target voltage with 0.96 ms. However, if a slower soft-start is required, an external capacitor can be tied from the ENx pin to GND. In this case, the TPS51220 charges the external capacitor with the integrated 2-µA current source. An approximate external soft-start time would be $t_{EX\text{-}SS} = C_{EX} / I_{EN12}$, which means the time from ENx = 1V to ENx = 2V. The recommend capacitance is more than 2.2nF.

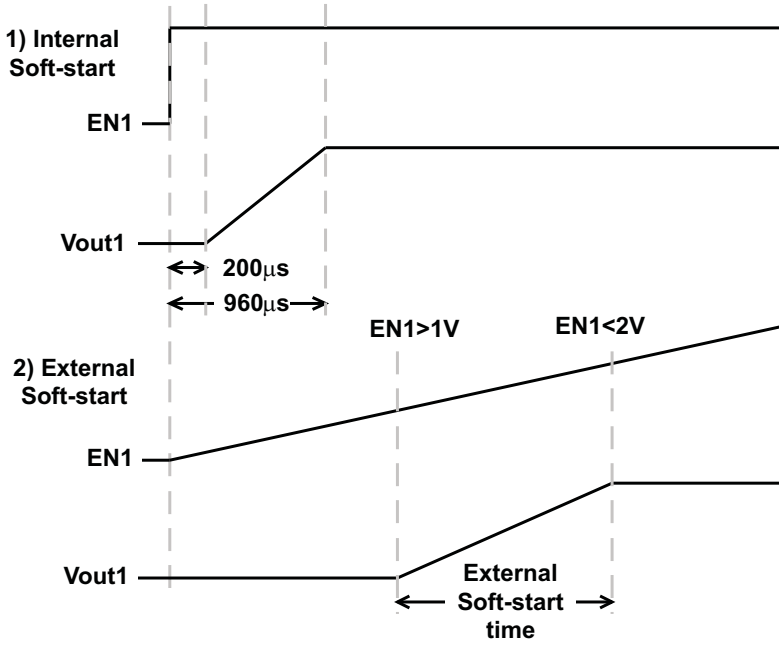


Figure 39. Enable and Soft-start Timing

Table 1. Enable Logic States

EN	EN1	EN2	VREG3	VREF2	VREG5	CH1	CH2
GND	Don't Care	Don't Care	**ON**	Off	Off	Off	Off
Hi	Lo	Lo	**ON**	**ON**	**ON**	Off	Off
Hi	Hi	Lo	**ON**	**ON**	**ON**	**ON**	Off
Hi	Lo	Hi	**ON**	**ON**	**ON**	Off	**ON**
Hi	Hi	Hi	**ON**	**ON**	**ON**	**ON**	**ON**

Pre-Biased Startup

The TPS51220 supports a pre-biased start up by preventing negative inductor current during soft-start in the condition the output capacitor has some charge. The initial DRVH signal waits until the voltage feedback signal becomes greater than the internal reference ramping up by soft-start function. After that, the start-up manner is the same as the way of fully discharged soft start condition. This manner is regardless of the SKIPSELx selection.

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3.3V, 10mA LDO (VREG3)

A 3.3-V, 10mA, linear regulator is integrated in the TPS51220. This LDO services some of the analog supply rail for the device and provides a handy standby supply for 3.3-V *Always On* voltage in the notebook system. Apply a 2.2-µF (at least 1-µF), high quality X5R or X7R ceramic capacitor from VREG3 to (signal) GND in adjacent to the device.

2V, 100µA Sink/ Source Reference (VREF2)

This voltage is used for the reference of the loop compensation network. Apply a 0.22-µF (at least 0.1-µF), high quality X5R or X7R ceramic capacitor from VREF2 to (signal) GND in adjacent to the device.

5.0V, 100mA LDO (VREG5)

A 5.0-V, 100mA, linear regulator is integrated in the TPS51220. This LDO services the main analog supply rail for the device and provides the current for gate drivers until switch-over function becomes enable. Apply a 10-µF (at least 4.7-µF), high quality X5R or X7R ceramic capacitor from VREG5 to (power) GND in adjacent to the device.

VREG5 SWITCHOVER

When EN1 is high, PGOOD1 indicates *GOOD* and more than 4.7 V is applied to V5SW, the internal 5-V LDO is shut off and the VREG5 is shorted to V5SW by an internal MOSFET after a 7.7-ms delay. When the V5SW voltage becomes lower than 4.5 V, EN1 becomes low, or PGOOD1 indicates BAD, the internal switch is turned off and the internal 5-V LDO resumes immediately

BASIC PWM OPERATIONS

The main control loop of the SMPS is designed as a fixed frequency, pulse width modulation (PWM) controller. It supports two control schemes; a peak current mode and a proprietary D-CAP mode. Current mode achieves stable operation in any type of capacitors including low ESR capacitor(s) such as ceramic or specialty polymer capacitors. D-CAP mode does not require an external compensation circuit, and is suitable for relatively larger ESR capacitor(s) configuration. These control schemes are selected with FUNC-pin; see Table 4.

CURRENT MODE

The current mode scheme uses the output voltage information and the inductor current information to regulate the output voltage. The output voltage information is sensed by VFBx pin. The signal is compared with the internal 1V reference and the voltage difference is amplified by a transconductance amplifier (VFB-AMP). The inductor current information is sensed by CSPx and CSNx pins. The voltage difference is amplified by another transconductance amplifier (CS-AMP). The output of the VFB-AMP indicates the target peak inductor current. If the output voltage goes down, the TPS51220 increases the target inductor current to raise the output voltage, on the other hand, if the output voltage goes up the TPS51220 decreases the target inductor current to reduce the output voltage.

At the beginning of each clock cycle, the high-side MOSFET is turned on, or becomes 'ON' state. The high-side MOSFET is turned off, or becomes *OFF* state, after the inductor current becomes the target value which is determined by the combination value of the output of the VFB-AMP and a ramp compensation signal. The ramp compensation signal is used to prevent sub-harmonic oscillation of the inductor current control loop. The high-side MOSFET is turned on again at the next clock cycle. By repeating the operation in this manner, the controller regulates the output voltage. The synchronous low-side or the *rectifying* MOSFET is turned on each *OFF* state to keep the conduction loss minimum.

D-CAP™ MODE

With the D-CAP mode operation, the PWM comparator compares VREF2 with the combination value of the COMP voltage, VFB-AMP output, and the ramp compensation signal. When the both signals are equal at the peak of the voltage sense signal, the comparator provides the *OFF* signal to the high-side MOSFET driver. Because the compensation network is implemented on the part and the output waveform itself is used as the error signal, external circuit is simplified. Another advantage is its inherent fast transient response. A trade-off is a sufficient amount of ESR required in the output capacitor. The D-CAP™ mode is suitable for relatively larger output ripple voltage application. The inductor current information is used for the overcurrent protection and light load operation.

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PWM FREQUENCY CONTROL

The TPS51220 has a fixed frequency control scheme with 180° phase shift. The switching frequency can be determined by an external resistor which is connected between RF pin and GND, and can be calculated using Equation 1.

$$f_{sw}\left[kHz\right] = \frac{1 \times 10^{5}}{RF\left[k\Omega\right]} \quad (1)$$

TPS51220 can also synchronize to more than 2.5-V amplitude external clock by applying the signal to the RF pin. The set timing of channel-1 initiates at the raising edge (1.3 V typ) of the clock and channel-2 initiates at the falling edge (1.1 V typ). Therefore, the 50% duty signal makes both channels 180° phase shift.

When the external clock synchronization is selected, the following actions are required.

- Remove RF resistor
- Add clock signal before EN1 or EN2 turning on.

TPS51220 can NOT support switching frequency change on the fly (from f_{SW} set by RF-resistor to ex-clock, nor vice versa).

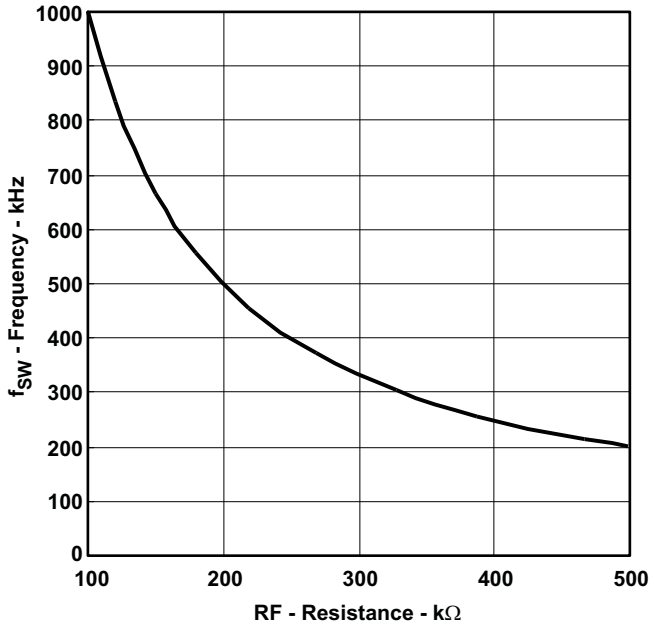

Figure 40. Switching Frequency vs RF

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LIGHT LOAD OPERATION

The TPS51220 automatically reduces switching frequency at light load condition to maintain high efficiency if *Auto Skip* or *Out-of-Audio* mode is selected by SKIPSELx. This reduction of frequency is achieved by skipping pulses. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to the point that its *peak* touches a predetermined current, $I_{LL(PEAK)}$, which indicates the boundary between heavy load and light load conditions. Once the top MOSFET is turned on, the TPS51220 does not allow it to be turned off until it touches $I_{LL(PEAK)}$. This eventually causes an overvoltage condition to the output and pulse skipping. From the next pulse after zero-crossing is detected, $I_{LL(PEAK)}$ is limited by the ramp down signal which starts from 25% of the overcurrent limit setting ($I_{OCL(PEAK)}$: see the current protection session) toward 5% of $I_{OCL(PEAK)}$ over one switching cycle to prevent causing large ripple. The transition load point to the light load operation $I_{LL(DC)}$ can be calculated as shown in Equation 2 and Equation 3.

$$I_{LL(DC)} = I_{LL(PEAK)} - 0.5 \times I_{IND(RIPPLE)} \quad (2)$$

$$I_{IND(RIPPLE)} = \frac{1}{L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (3)$$

where

- f_{SW} is the PWM switching frequency which is determined by RF resistor setting or external clock

Switching frequency versus output current in the light load condition is a function of L, f, V_{IN} and V_{OUT}, but it decreases almost proportional to the output current from the $I_{LL(DC)}$ given above; however, as the switching is synchronized with clock. Due to the synchronization, the switching waveform in boundary load condition (close to $I_{LL(DC)}$) appears as a sub-harmonic oscillation; however, it is the intended operation.

If SKIPSELx is tied to GND, the TPS51220 works on a constant frequency of f_{SW} regardless its load current.

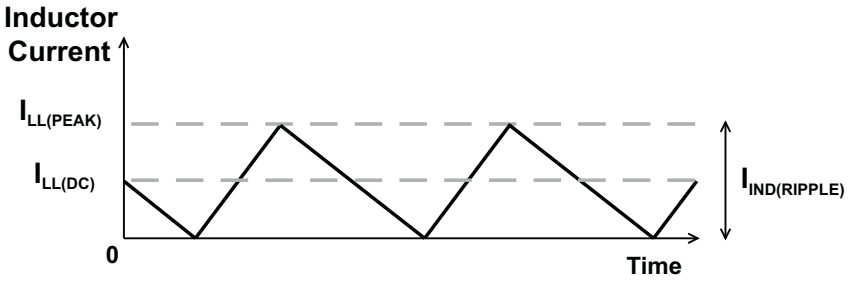

Figure 41. Boundary Between Pulse Skipping and CCM

$$I_{LL(PEAK)Ramp} = (0.25\text{-}0.2 \times \frac{V_{OUT}}{V_{IN}}) \times I_{OCL(PEAK)} \quad (4)$$

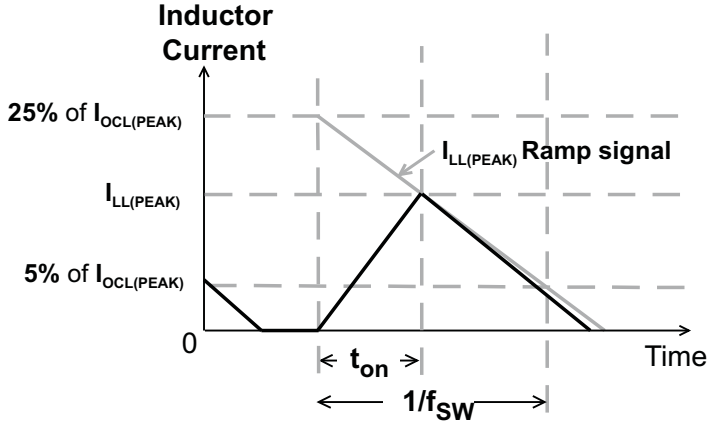

Figure 42. Inductor Current Limit at Pulse Skipping

Table 2. Skip Mode Selection

SKIPSELx	GND	VREF2	VREG3	VREG5
OPERATING MODE	Continuous Conduction	Auto Skip	OOA Skip (max 7 skips, for <400 kHz)	OOA Skip (max 15 skips, for equal to or greater than 400kHz)

OUT OF AUDIO SKIP OPERATION

Out-Of-Audio™ (OOA) light load mode is a unique control feature that keeps the switching frequency above acoustic audible frequencies toward virtually no load condition while maintaining best of the art high conversion efficiency. When OOA is selected, the switching frequency is kept higher than audible frequency range in any load condition. The TPS51220 automatically reduce switching frequency at a light load condition. OOA control circuit monitors the states of both MOSFETs and forces *ON* state if predetermined number of pulses are skipped. This means that the high-side MOSFET is turned on before the output voltage declines down to the target value, so that eventually an overvoltage condition is caused. The OOA control circuit detects this overvoltage condition and begins modulating the skip-mode on time to keep the output voltage.

TPS51220 supports wide switching frequency range; therefore, the OOA skip mode has two selections, see Table 2. When 300kHz switching frequency is selected, max 7 skip (SKIPSEL=3.3V) makes the lowest frequency at 37.5kHz. If max 15 skip is chosen, it becomes 18.8kHz, hence max 7 skip is suitable for less than 400kHz, and max 15 skip is for equal to or greater than 400kHz.

99% DUTY CYCLE OPERATION

In a low dropout condition such as 5V input to 5V output, the basic control loop tries to keep the high-side MOSFET 100% *ON* as a nature. However, with N-MOSFET used for the top switch, it is not possible to use the 100% on cycle to charge the boot strap capacitor. TPS51220 detects the 100% *ON* condition and inserts the *OFF* state at the appropriate time. When high duty is required, TPS51220 extends the ON period (skips maximum 3 clock cycles which means f_{SW} becomes 1/4 of the setting number at steady state) and asserts the OFF state after extended ON.

HIGH-SIDE DRIVER

The high-side driver is designed to drive high current, low $r_{DS(on)}$ N-channel MOSFET(s). The drive capability is represented by its internal resistance, which is 1.7Ω for VBSTx to DRVHx, and 1Ω for DRVHx to SWx. When configured as a floating driver, 5V bias voltage is delivered from VREG5 supply. The instantaneous drive current is supplied by the flying capacitor between VBSTx and SWx pins. The average drive current is equal to the gate charge at Vgs = 5V times switching frequency. This gate drive current as well as the low-side gate drive current times 5V makes the driving power which needs to be dissipated from TPS51220 package. A dead time to prevent shoot through is internally generated between high-side MOSFET off to low-side MOSFET on, and low-side MOSFET off to high-side MOSFET on.

LOW-SIDE DRIVER

The low-side driver is designed to drive high current low $r_{DS(on)}$ N-channel MOSFET(s). The drive capability is represented by its internal resistance, which are 1.3Ω for VREG5 to DRVLx and 0.7Ω for DRVLx to GND. The 5V bias voltage is delivered from VREG5 supply. The instantaneous drive current is supplied by an input capacitor connected between VREG5 and GND. The average drive current is also calculated by the gate charge at Vgs = 5V times switching frequency.

CURRENT SENSING SCHEME

In order to provide both good accuracy and cost effective solution, the TPS51220 supports external resistor sensing and inductor DCR sensing. An RC network with high quality X5R or X7R ceramic capacitor should be used to extract voltage drop across DCR. 0.1µF is a good value to start the design. CSPx and CSNx should be connected to positive and negative terminal of the sensing device respectively. TPS51220 has an internal current amplifier. The gain of the current amplifier, *Gc*, is selected by TRIP terminal. In any setting, the output signal of the current amplifier becomes 100mV at the OCL setting point. This means that the current sensing amplifier normalize the current information signal based on the OCL setting. Attaching a RC network recommended even with a resistor sensing scheme to get an accurate current sensing; see the external parts selection session for detailed configurations.

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CURRENT PROTECTION

TPS51220 has cycle-by-cycle overcurrent limiting control. If the inductor current becomes larger than the overcurrent trip level, TPS51220 turns off high-side MOSFET, turns on low-side MOSFET and waits for the next clock cycle.

$I_{OCL(PEAK)}$ sets peak level of the inductor current. Thus, the dc load current at overcurrent threshold, $I_{OCL(DC)}$, can be calculated as shown in Equation 5 and Equation 6.

$$I_{OCL(DC)} = I_{OCL(PEAK)} - 0.5 \times I_{IND(RIPPLE)} \quad (5)$$

$$I_{OCL(PEAK)} = \frac{V_{OCL}}{R_{SENSE}}$$

where

- R_{SENSE} is resistance of current sensing device
- $V_{(OCL)}$ is overcurrent trip threshold voltage which is determined by TRIP pin voltages as shown in Table 3. (6)

In an overcurrent condition, the current to the load exceeds the current to the output capacitor thus the output voltage tends to fall down, and it will end up with crossing the undervoltage protection threshold and shutdown.

Table 3. OCL Trip and Discharge Selection

TRIP	GND	VREF2	VREG3	VREG5
$V_{(OCL)}$ (OCL Trip voltage)	$V_{(OCL-ULV)}$ (Ultra Low Voltage)		$V_{(OCL-LV)}$ (Low Voltage)	
Discharge	Enable	Disable	Disable	Enable

POWERGOOD

The TPS51220 has powergood output for both switcher channels. The powergood function is activated after softstart has finished. If the output voltage becomes within ±5% of the target value, internal comparators detect power good state and the powergood signal becomes high after 1ms internal delay. If the output voltage goes outside of ±10% of the target value, the powergood signal becomes low after 1.5µs internal delay. Apply voltage should be less than 6V and the recommended pull-up resistance value is from 100kΩ to 1MΩ.

OUTPUT DISCHARGE CONTROL

The TPS51220 discharges output when ENx is low. The TPS51220 discharges outputs using an internal MOSFET which is connected to CSNx and GND. The current capability of these MOSFETs is limited to discharge the output capacitor slowly. If ENx becomes high during discharge, MOSFETs are turning off, and some output voltage remains. SMPS changes over to soft-start. PWM will begin after the target voltage overtakes the remaining output voltage. This function can be disabled as shown in Table 3.

OVER/UNDERVOLTAGE PROTECTION

TPS51220 monitors the output voltage to detect over and undervoltage. When the output voltage becomes 15% higher than the target value, the OVP comparator output goes high and the circuit latches as the high-side MOSFET driver OFF and the low-side MOSFET driver ON, and shuts off another channel.

When the feedback voltage becomes lower than 70% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 1ms, TPS51220 latches OFF both high-side and low-side MOSFETs, and shuts off another channel. This UVP function is enabled after soft start has completed. OVP function can be disabled as Table 4. The procedures for restarting from these protection states are:

1. toggle EN
2. toggle EN1 and EN2 or
3. once hit UVLO

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Table 4. FUNC Logic States

FUNC	GND	VREF2	VREG3	VREG5
OVP	Enable	Disable	Enable	Disable
Control Scheme	Current mode	D-CAP mode	D-CAP mode	Current mode

UVLO PROTECTION

TPS51220 has undervoltage lock out protections (UVLO) for VREG5, VREG3 and VREF2. When the voltage is lower than UVLO threshold voltage, TPS51220 shuts off each output as Table 5. This is non-latch protection.

Table 5. UVLO Protection

	CH1/ CH2	VREG5	VREG3	VREF2
VREG5 UVLO	Off	—	On	On
VREG3 UVLO	Off	Off	—	Off
VREF2 UVLO	Off	Off	On	—

THERMAL SHUTDOWN

TPS51220 monitors the temperature of itself. If the temperature exceeds the threshold value, TPS51220 shuts off both SMPS and 5V-LDO, and decreases the VREG3 current limitation to 5 mA (typically). This is non-latch protection.

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APPLICATION INFORMATION

EXTERNAL PARTS SELECTION

A buck converter using TPS51220 consists of linear circuits and a switching modulator. Figure 43 and Figure 44 show basic scheme.

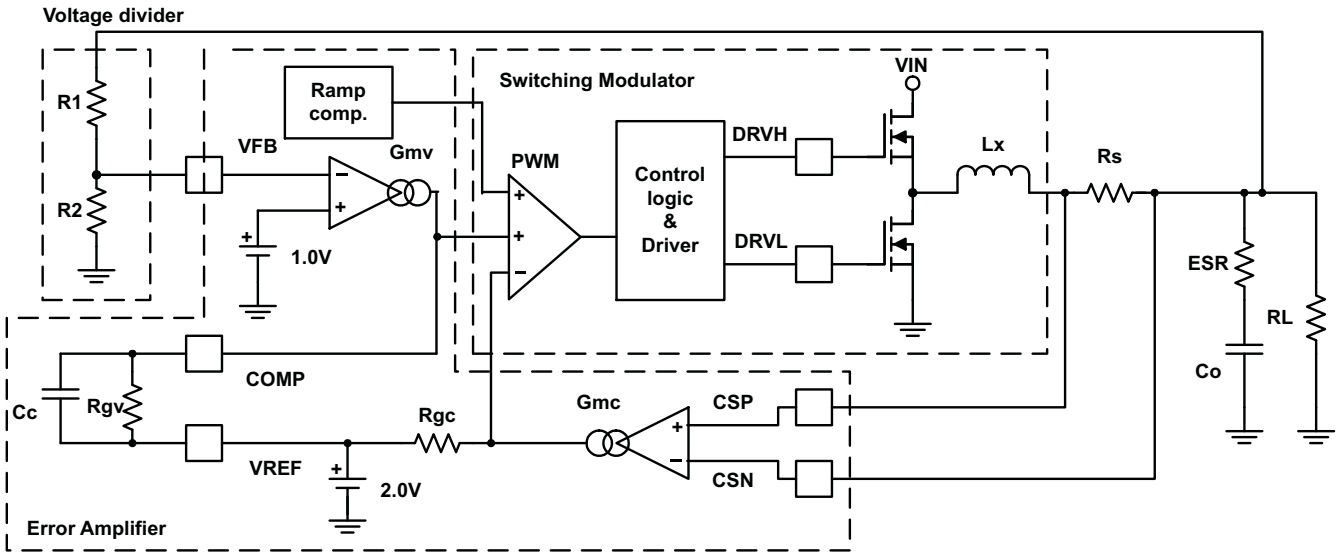

Figure 43. Simplified Current Mode Functional Blocks

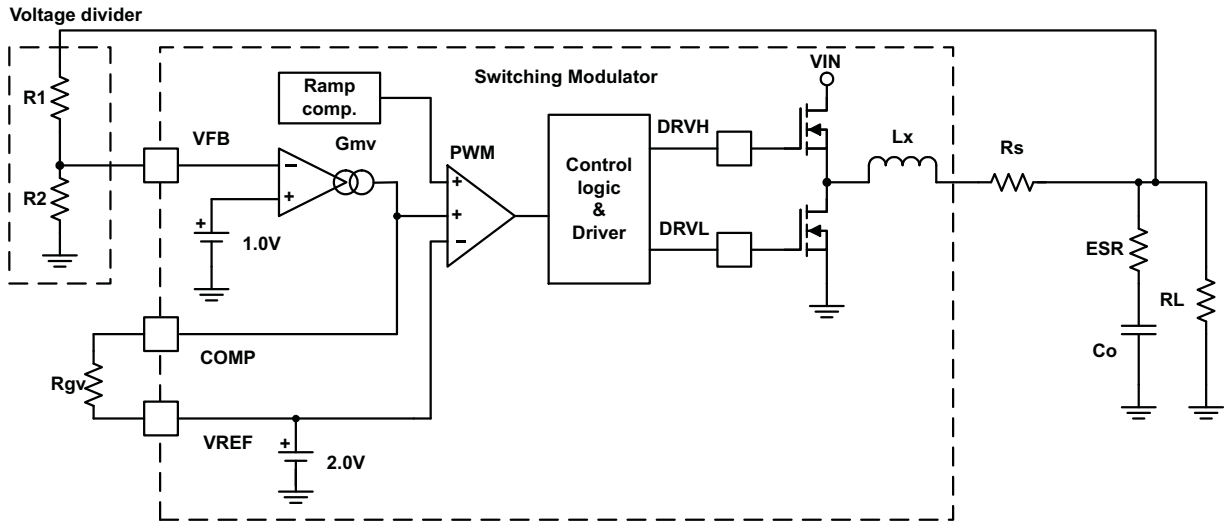

Figure 44. Simplified D-CAP Mode Functional Blocks

The external components can be selected by following manner.

1. Determine output voltage dividing resistors (R1 and R2: shown in Figure 43) using the next equation

$$R1 = \left(V_{OUT} - 1.0\right) \times R2 \quad (7)$$

   For D-CAP mode, recommended R2 value is from 10 kΩ to 20 kΩ.

2. **Determine switching frequency.** Higher frequency allows smaller output capacitances, however, degrade efficiency due to increase of switching loss. Frequency setting resistor for RF-pin can be calculated by;

$$RF[k\Omega] = \frac{1 \times 10^5}{f_{sw}\,[kHz]} \quad (8)$$

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3. **Choose the inductor.** The inductance value should be determined to give the ripple current of approximately 25% to 50% of maximum output current. Recommended ripple current rate is approximately 30% to 40% at the typical input voltage condition, next equation uses 33%.

$$L = \frac{1}{0.33 \times I_{OUT(MAX)} \times f_{SW}} \times \frac{(V_{IN(TYP)} - V_{OUT}) \times V_{OUT}}{V_{IN(TYP)}} \quad (9)$$

The inductor also needs to have low DCR to achieve good efficiency, as well as enough room above peak inductor current before saturation.

4. Determine the OCL trip voltage threshold, $V_{(OCL)}$, and select the sensing resistor.

The OCL trip voltage threshold is determined by TRIP pin setting. To use larger value improves S/N ratio. Determine the sensing resistor using next equation. $I_{OCL(PEAK)}$ should be approximately 1.5 × $I_{OUT(MAX)}$ to 1.7 × $I_{OUT(MAX)}$.

$$R_{SENSE} = \frac{V_{OCL}}{I_{OCL(PEAK)}} \quad (10)$$

5. **Determine Rgv.** Rgv should be determined from preferable droop compensation value and is given by next equation based on the typical number of Gmv = 500 µS.

$$Rgv = 0.1 \times \frac{I_{OUT(MAX)}}{I_{OCL(PEAK)}} \times V_{OUT} \times \frac{1}{Gmv \times Vdroop} \quad (11)$$

$$Rgv[k\Omega] = 200 \times \frac{I_{OUT(MAX)}}{I_{OCL(PEAK)}} \times \frac{V_{OUT}[V]}{Vdroop[mV]} \quad (12)$$

For D-CAP mode, Rgv is used for adjusting ramp compensation. 10kΩ is a good value to start design with. 6kΩ to 20kΩ can be chosen.

6. Determine output capacitance *Co* to achieve a stable operation using the next equation. The 0 dB frequency, f_o, should be kept under 1/3 of the switching frequency.

$$f_0 = \frac{5}{\pi} \times I_{OCL(PEAK)} \times \frac{1}{V_{OUT}} \times \frac{Gmv \times Rgv}{Co} < \frac{fsw}{3} \quad (13)$$

$$Co > \frac{15}{\pi} \times I_{OCL(PEAK)} \times \frac{1}{V_{OUT}} \times \frac{Gmv \times Rgv}{fsw} \quad (14)$$

For D-CAP mode, f_o is determined by the output capacitor's characteristics as below.

$$f_0 = \frac{1}{2\pi \times ESR \times Co} < \frac{fsw}{3} \quad (15)$$

$$Co > \frac{3}{2\pi \times ESR \times fsw} \quad (16)$$

For better jitter performance, a sufficient amount of feedback signal is required at VFBx pin. The recommended signal level is approximately 30 mV per t_{sw} (switching period) of the ramping up rate, and more than 4 mV of peak-to-peak voltage.

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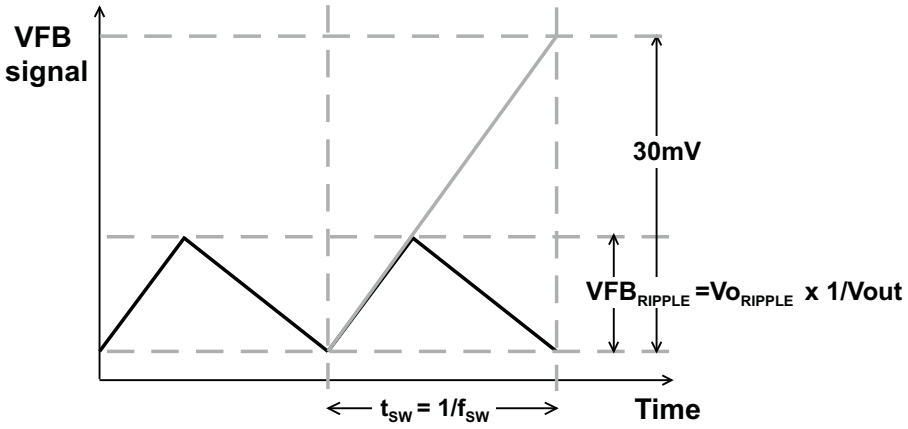

Figure 45. Required voltage feedback ramp signal

7. **Calculate Cc.** The purpose of this capacitance is to cancel zero caused by *ESR* of the output capacitor. If ceramic capacitor(s) is used, there is no need for Cc. If a combination of different capacitors is used, attach a RC network circuit instead of single capacitance to cancel zeros and poles caused by the output capacitors. With single capacitance, Cc is given in Equation 17.

$$Cc = Co \times \frac{ESR}{Rgv} \tag{17}$$

   For D-CAP mode, basically Cc is not needed.

8. **Choose MOSFETs** Generally, the on resistance affects efficiency at high load conditions as conduction loss. For a low output voltage application, the duty ratio is not high enough so that the on resistance of high-side MOSFET does not affect efficiency; however, switching speed (t_r and t_f) affects efficiency as switching loss. As for low-side MOSFET, the switching loss is usually not a main portion of the total loss.

RESISTOR CURRENT SENSING

For more accurate current sensing with an external resistor, the following technique is recommended. Adding an RC filter to cancel the parasitic inductance of resistor, this filter value is calculated using Equation 18.

$$Cx \times Rx = \frac{Lx}{Rs} \tag{18}$$

This equation means time-constant of Cx and Rx should match the one of Lx (ESL) and Rs.

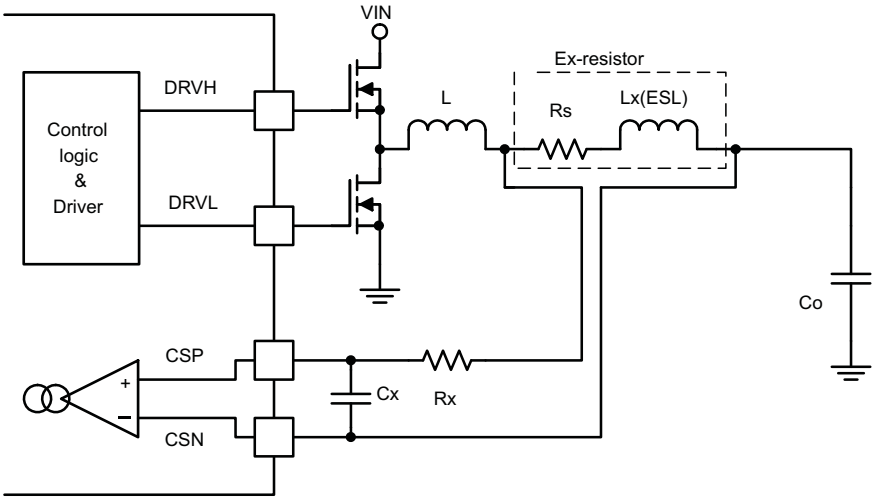

Figure 46. External Resistor Current Sensing

INDUCTOR DCR CURRENT SENSING

To use inductor DCR as current sensing resistor (Rs), the configuration needs to change as below. However, the equation must be satisfied is the same as the one of resistor sensing.

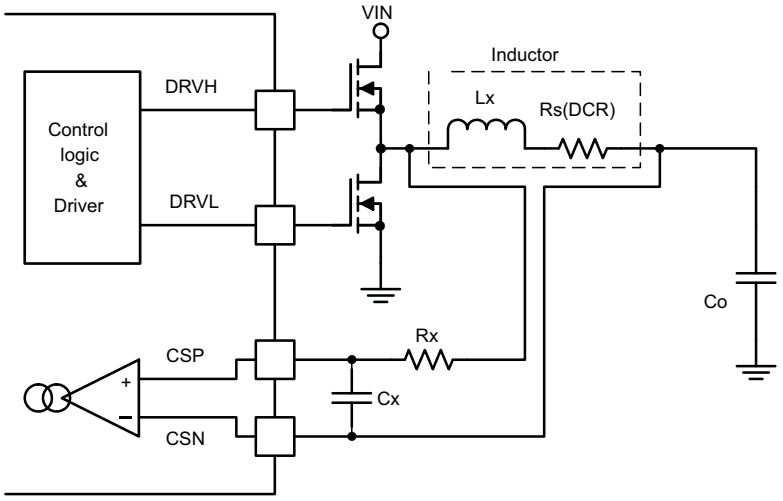

Figure 47. Inductor DCR Current Sensing

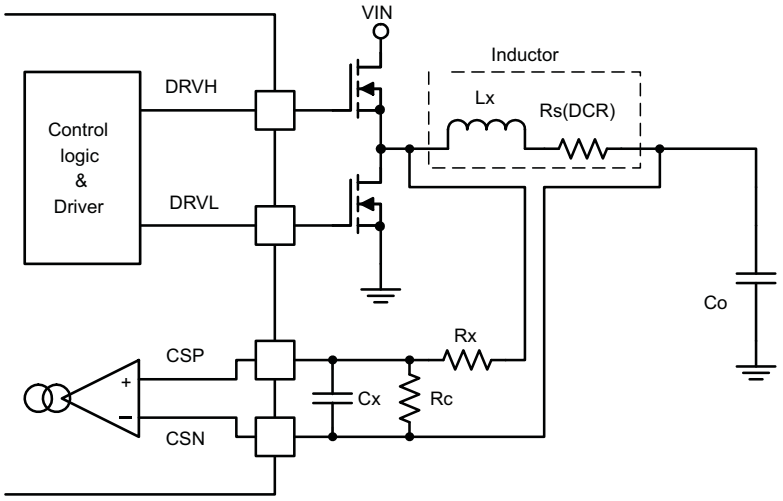

Figure 48. Inductor DCR Current Sensing With Voltage Divider

TPS51220 has fixed $V_{(OCL)}$ point (60 mV or 30 mV). In order to adjust for DCR, a voltage divider can be configured as Figure 48.

For Rx, Rc and Cx can be calculated as shown in Equation 20, and overcurrent limitation value can be calculated in Equation 20.

$$Cx \times (Rx // Rc) = \frac{Lx}{Rs} \tag{19}$$

$$I_{OCL(PEAK)} = V_{OCL} \times \frac{1}{Rs} \times \frac{Rx + Rc}{Rc} \tag{20}$$

Figure 49 shows the compensation technique for the temperature drifts of the inductor DCR value. This scheme assumes the temperature rise at the thermistor (R_{NTC}) is directly proportional to the temperature rise at the inductor.

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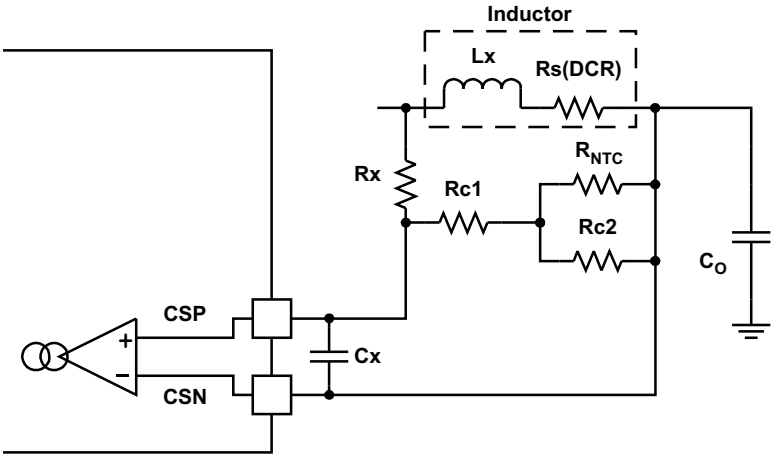

Figure 49. Inductor DCR Current Sensing With Temperature Compensate

LAYOUT CONSIDERATIONS

Certain points must be considered before starting a PCB layout work using the TPS51220.

Placement

- Place RC network for CSP1 and CSP2 close to the device pins.
- Place bypass capacitors for VREG5, VREG3 and VREF2 close to the device pins.
- Place frequency-setting resistor close to the device pin.
- Place the compensation circuits for COMP1 and COMP2 close to the device pins.
- Place the voltage setting resistors close to the device pins, especially when D-CAP mode is chosen.

Routing (sensitive analog portion)

- Use separate traces for; see Figure 50
  - Output voltage sensing from current sensing (negative-side)
  - Output voltage sensing from V5SW input (when V_{OUT} = 5V)
  - Current sensing (positive-side) from switch-node

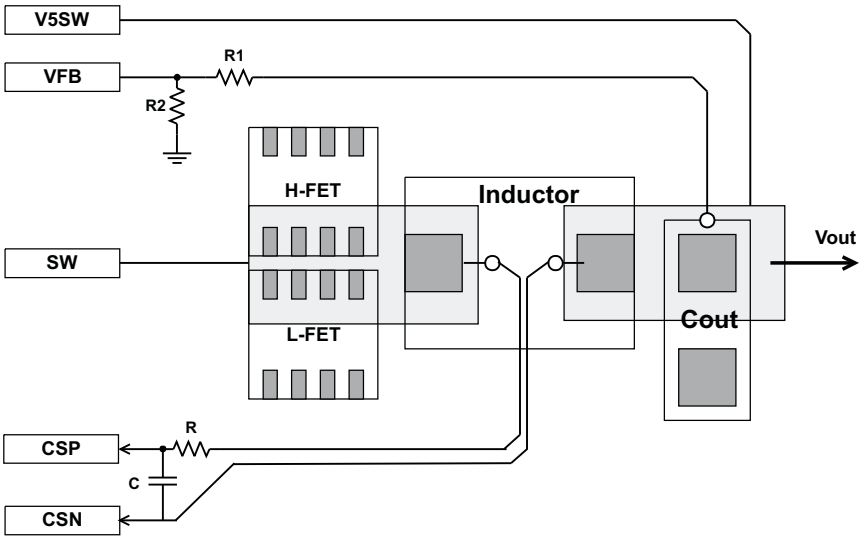

Figure 50. Sensing Trace Routings

- Use Kelvin sensing traces from the solder pads of the current sensing device (inductor or resistor) to current

sensing comparator inputs (CSPx and CSNx). (See Figure 51)

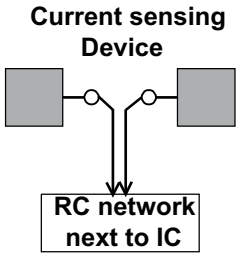

Figure 51. Current Sensing Traces

- Use small copper space for VFBx. These are short and narrow traces to avoid noise coupling
- Connect VFB resistor trace to the positive node of the output capacitor.
- Use signal GND for VREF2 and VREG3 capacitors, RF and VFB resistors, and the other sensitive analog components. Placing a signal GND plane (underneath the device, and fully covered peripheral components) on the internal layer for shielding purpose is recommended. (See Figure 52)
- Use a thermal land for PowerPAD™. Five or more vias, with 0.33-mm (13-mils) diameter connected from the thermal land to the internal GND plane, should be used to help dissipation. Do NOT connect the GND-pin to this thermal land on the surface layer, underneath the package.

Routing (power portion)

- Use wider/ shorter traces of DRVL for low-side gate drivers to reduce stray inductance.
- Use the parallel traces of SW and DRVH for high-side MOSFET gate drive, and keep them away from DRVL.
- Connect SW trace to source terminal of the high-side MOSFET.
- Use power GND for VREG5, VIN and Vout capacitors and low-side MOSFETs. Power GND and signal GND should be connected near the device GND terminal. (See Figure 52)

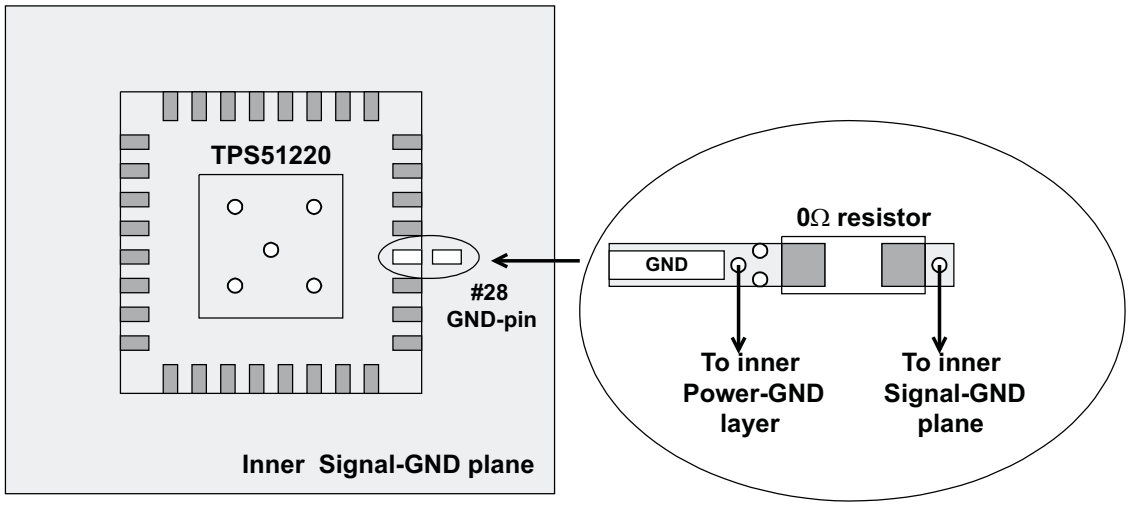

Figure 52. GND Layout Example

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APPLICATION CIRCUITS

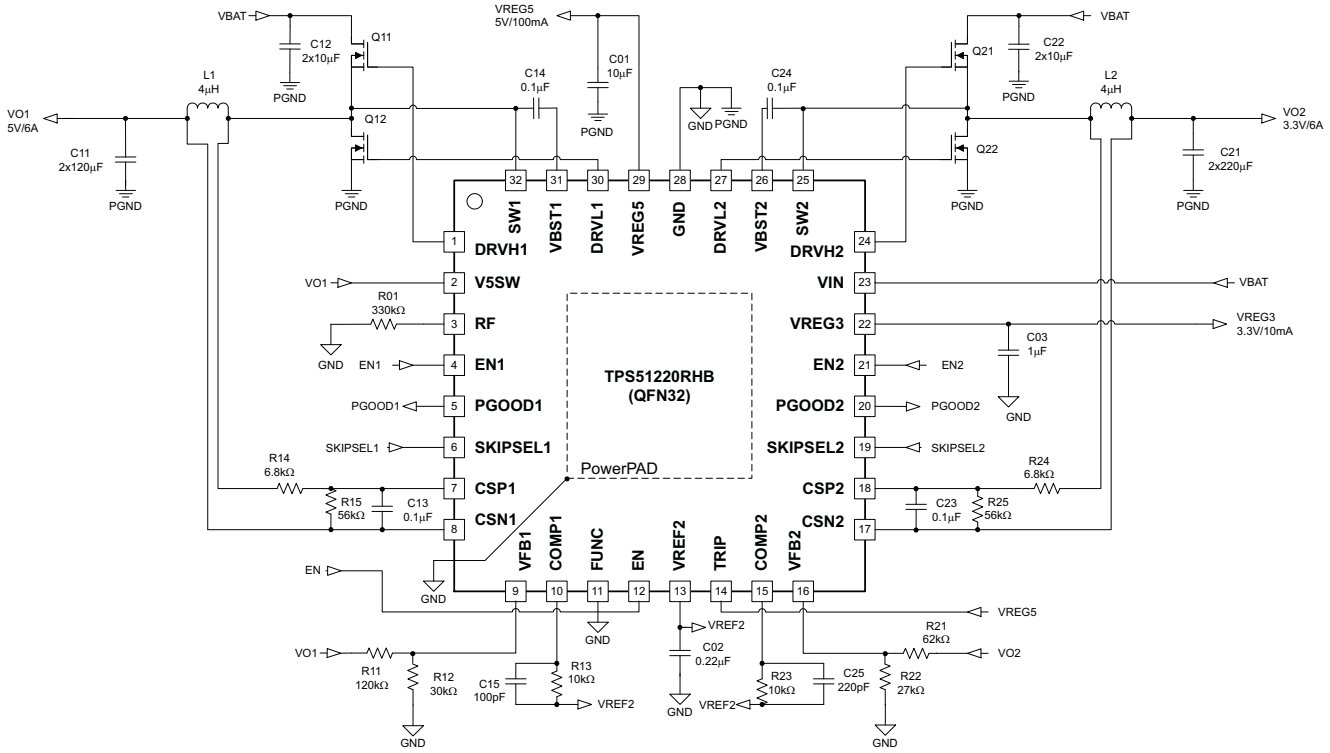

Figure 53. Current Mode, DCR Sensing, 5.0V/5A, 3.3V/5A, 300-kHz

Table 6. Current Mode, DCR Sensing, 5.0V/5A, 3.3V/5A, 300-kHz

SYMBOL	SPECIFICATION	MANUFACTURER	PART NUMBER
C11	2 × 120 µF/ 6.3 V/15-mΩ	Panasonic	EEFCX0J121R
C12	2 × 10 µF/ 25 V	Murata	GRM32DR71E106K
C21	2 × 220 µF/ 4.0 V/15-mΩ	Panasonic	EEFCX0G221R
C22	2 × 10 µF/ 25 V	Murata	GRM32DR71E106K
L1	4.0 µH, 10.3 A, 6.6-mΩ	Sumida	CEP125-4R0MC-H
L2	4.0 µH, 10.3A, 6.6-mΩ	Sumida	CEP125-4R0MC-H
Q11, Q21	30-V, 13.6-A, 9.5-mΩ	IR	IRF7821
Q12, Q22	30-V, 13.8-A, 5.8-mΩ	IR	IRF8113

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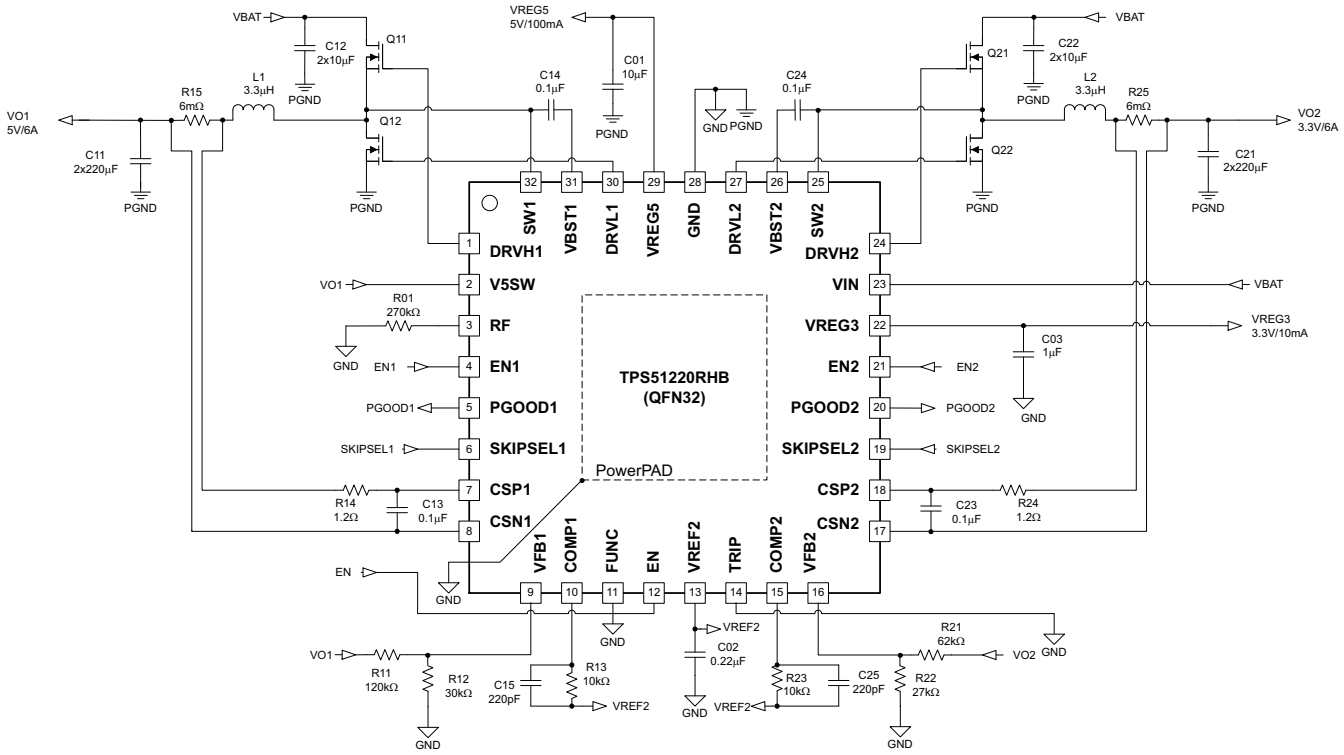

Figure 54. Current Mode, Ex-Resistor Sensing, 5.0V/5A, 3.3V/5A, 370-kHz

Table 7. Current Mode, Ex-Resistor Sensing, 5.0V/5A, 3.3V/5A, 370-kHz

SYMBOL	SPECIFICATION	MANUFACTURER	PART NUMBER
C11	2 x 220 µF/ 6.3 V/12-mΩ	Panasonic	EEFUE0J221R
C12	2 x 10 µF/ 25 V	Murata	GRM32DR71E106K
C21	2 x 220 µF/ 4.0 V/12-mΩ	Panasonic	EEFUE0G221R
C22	2 x 10 µF/ 25 V	Murata	GRM32DR71E106K
L1	3.3 µH, 10.3 A, 5.9-mΩ	TOKO	FDA1055-3R3M
L2	3.3 µH, 10.3 A, 5.9-mΩ	TOKO	FDA1055-3R3M
Q11, Q21	30-V, 13.6-A, 9.5-mΩ	IR	IRF7821
Q12, Q22	30-V, 13.8-A, 5.8-mΩ	IR	IRF8113

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REVISION HISTORY

Changes from Original (October 2007) to Revision A **Page**

- Changed the $t_{(SSDYL)}$ TYP Value From: 140 To: 200 6
- Changed the $t_{(SS)}$ TYP value From: 800 To: 960 6
- Changed text in the Enable and Soft Start section From: "ramps up the output voltage from zero to the target voltage with 0.8 ms" To: ramps up the output voltage from zero to the target voltage with 0.96 ms" 20
- Changed Figure 39 to show the softstart 960 µs delay 20

Changes from Revision A (November 2007) to Revision B **Page**

- Changed SW1, SW2 value in ABSOLUTE MAXIMUM RATINGS table from "–2 to 30" to "–5 to 30" 3
- Changed V5SW value in ABSOLUTE MAXIMUM RATINGS table from "–0.3 to 7" to " –1 to 7" 3
- Changed DRVH1, DRVH2 value in ABSOLUTE MAXIMUM RATINGS table from "–2 to 35" to " –5 to 35" 3
- Changed the RECOMMENDED OPERATING CONDITIONS table 3
- Added section: Pre-Biased Startup 20

Changes from Revision B (March 2009) to Revision C **Page**

- Changed SW1, SW2 value in ABSOLUTE MAXIMUM RATINGS table from: "–5 to 30" to "–7 to 30" 3
- Changed V5SW value in ABSOLUTE MAXIMUM RATINGS table from "–1 to 7" to "–7 to 7" 3
- Changed DRVH1, DRVH2 value in ABSOLUTE MAXIMUM RATINGS table from "–5 to 35" to "–7 to 35" 3

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS51220RHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	TPS 51220
TPS51220RHBR.A	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 51220
TPS51220RHBR.B	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 51220
TPS51220RHBRG4	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 51220
TPS51220RHBRG4.A	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 51220
TPS51220RHBRG4.B	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 51220
TPS51220RHBT	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	TPS 51220
TPS51220RHBT.A	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 51220
TPS51220RHBT.B	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 51220

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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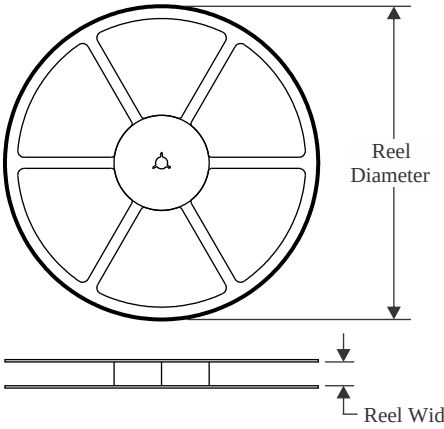
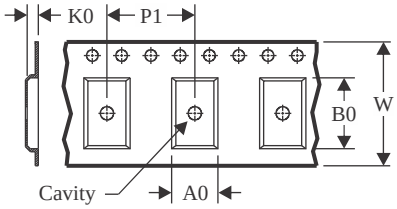
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

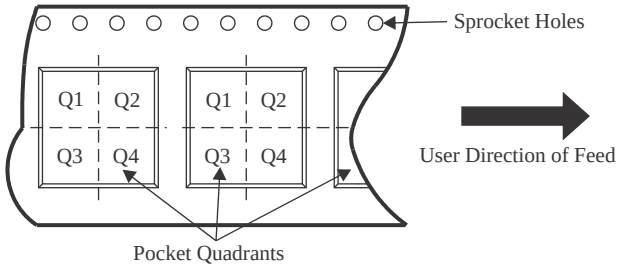


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

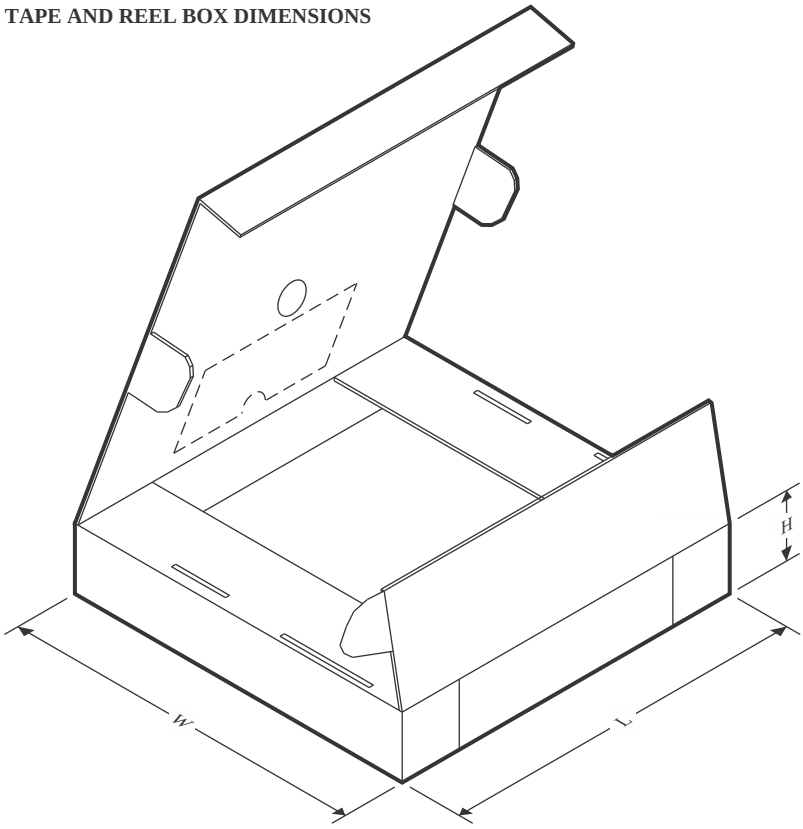
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51220RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS51220RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS51220RHBR	VQFN	RHB	32	3000	330.0	12.4	5.25	5.25	1.1	8.0	12.0	Q2
TPS51220RHBRG4	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS51220RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51220RHBR	VQFN	RHB	32	3000	353.0	353.0	32.0
TPS51220RHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
TPS51220RHBR	VQFN	RHB	32	3000	367.0	367.0	38.0
TPS51220RHBRG4	VQFN	RHB	32	3000	367.0	367.0	35.0
TPS51220RHBT	VQFN	RHB	32	250	210.0	185.0	35.0

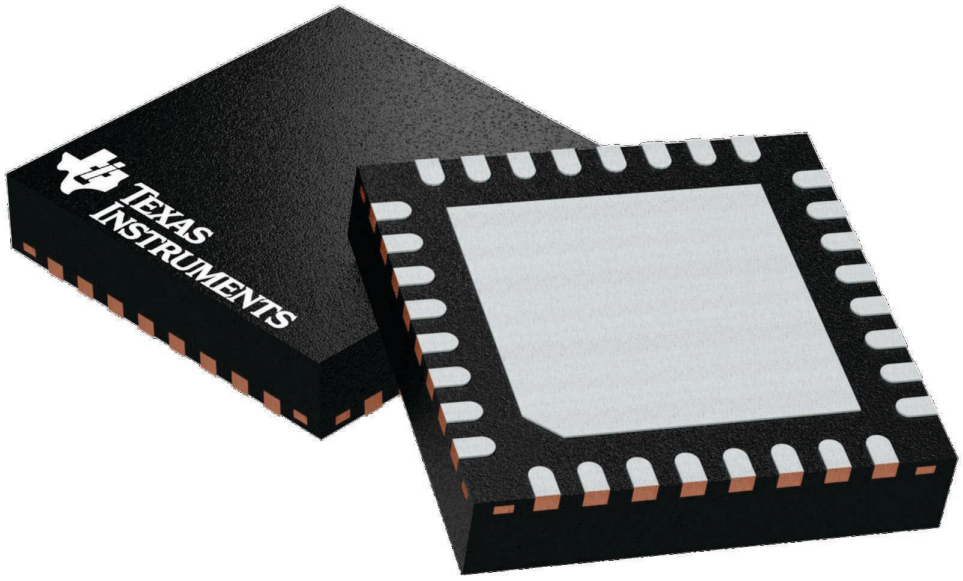
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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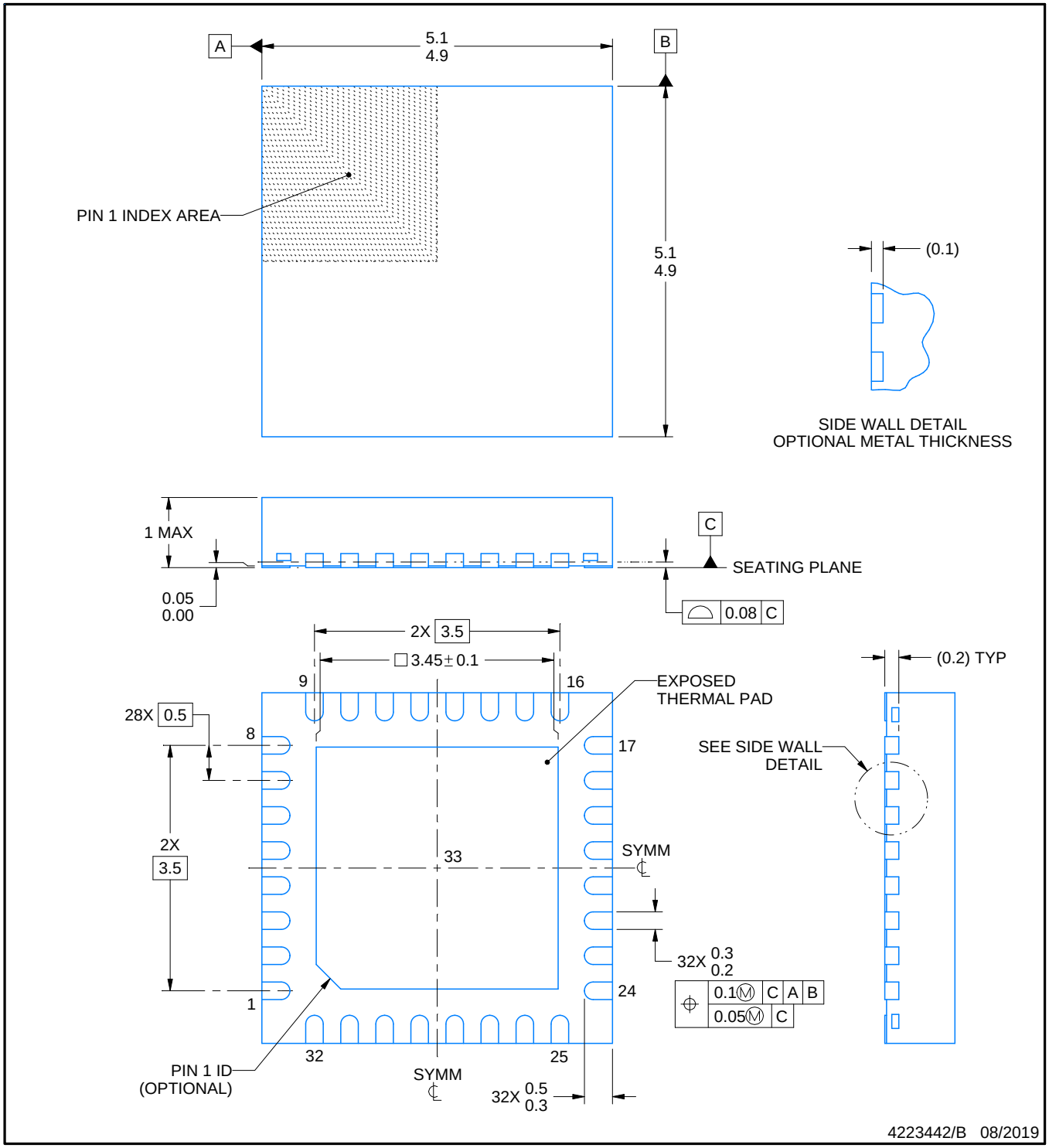
RHB0032E

PACKAGE OUTLINE

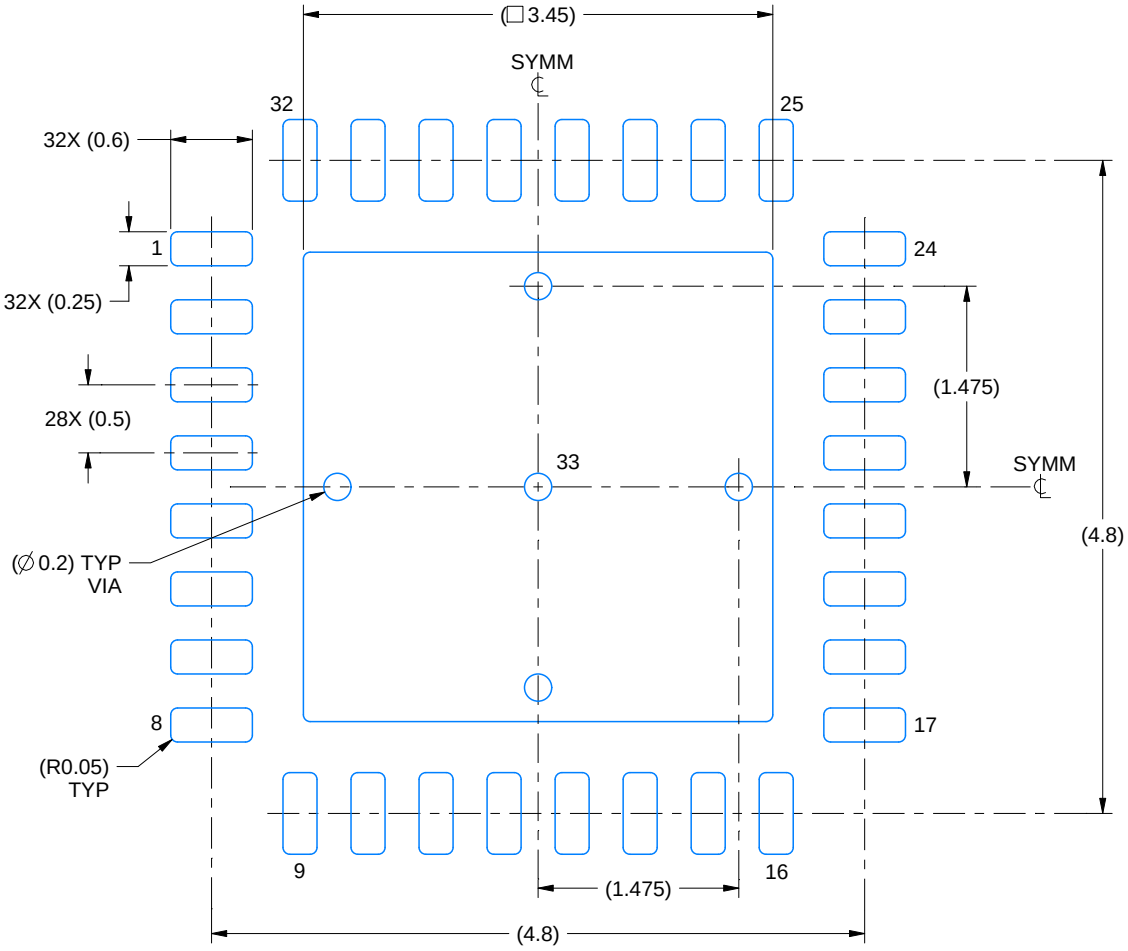
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

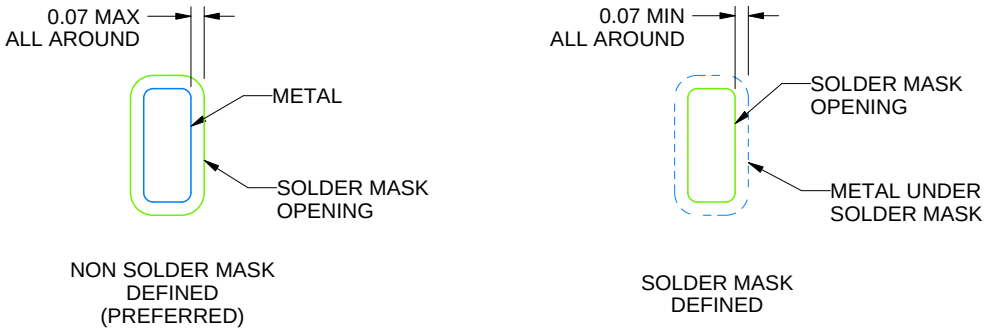


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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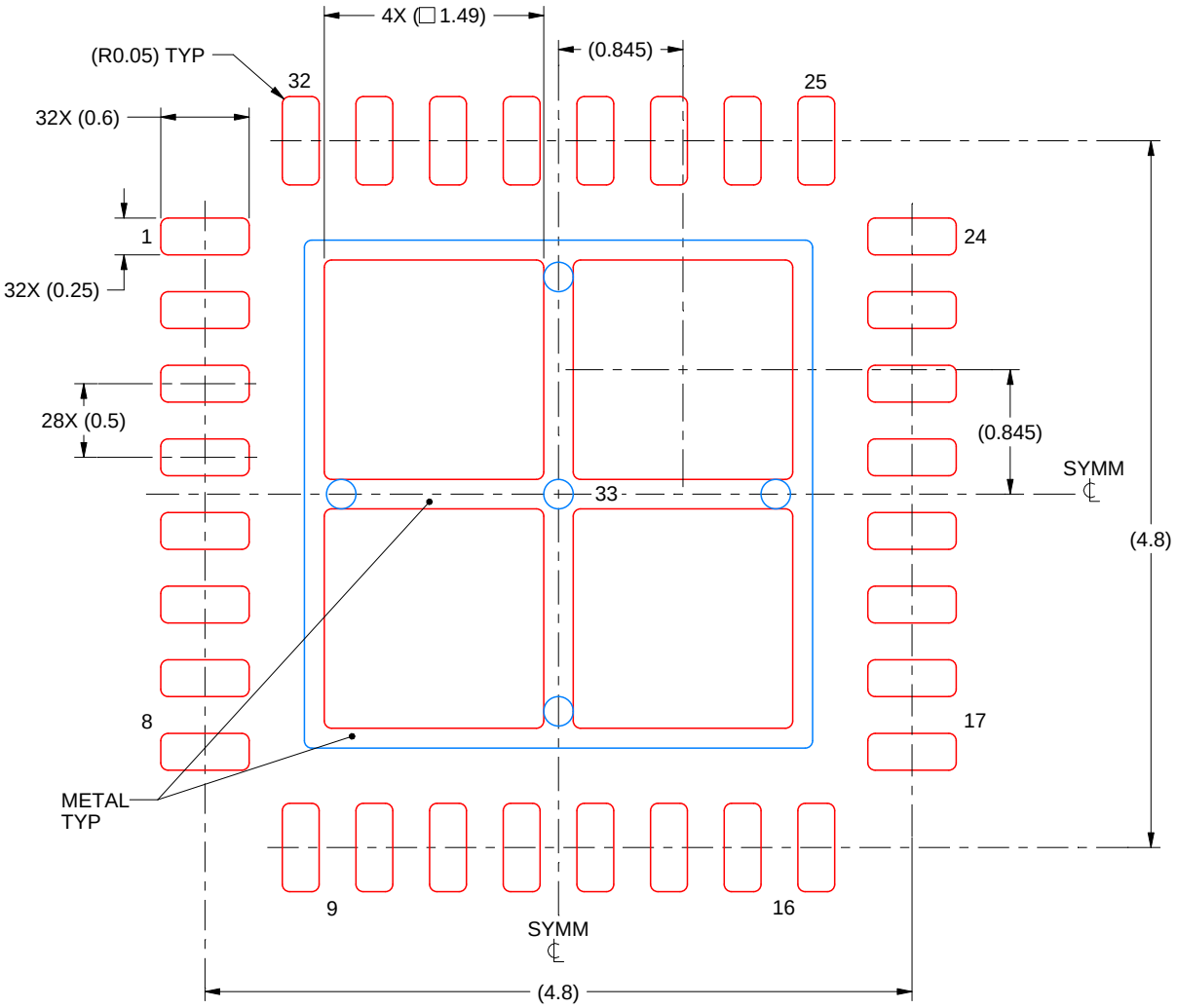
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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