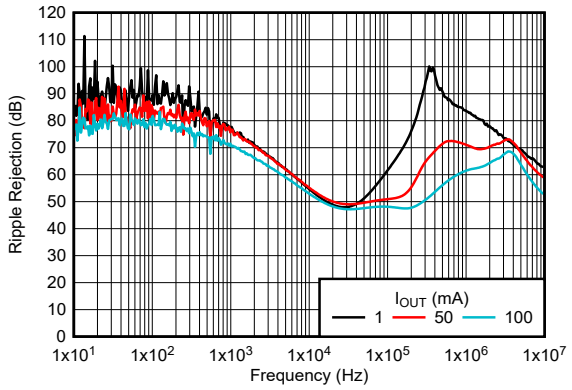
# TPS769 100mA, 16V, Low-Dropout Linear Regulator

## 1 Features

- Input voltage range:
  - Legacy chip: 2.7V to 10V (13.5V absolute max)
  - New chip: 2.5V to 16V (18V absolute max)
- Output voltage range (adjustable):
  - Legacy chip: 1.25V to 5.5V
  - New chip: 1.2V to 5.5V
- Output voltage range (fixed):
  - Legacy chip: 1.5V to 5V
  - New chip: 1.2V to 5V
- Maximum output current: Up to 100mA
- High PSRR (new chip): 46dB at 1MHz
- Output accuracy:
  - Legacy chip: 3% over load and temperature
  - New chip: 1.2% over load and temperature
- Dropout voltage:
  - Legacy chip: 71mV (typ) at 100mA (TPS76950)
  - New chip: 215mV (typ) at 100mA (TPS76950)
- Integrated fault protection:
  - Thermal shutdown
  - Overcurrent protection
- Internal soft-start time (new chip): 750µs (typical)
- Output capacitor for stable operation:
  - Legacy chip: ≥ 4.7µF
  - New chip: ≥ 2.2µF
- Package:
  - 5-pin SOT-23, $R_{\theta JA}$ = 178.6°C/W (new chip)

## 2 Applications

- Residential air conditioners
- HVAC systems
- Washers and dryers
- Industrial transportation




**TPS76933 PSRR vs Output Current (New Chip)**

## 3 Description

The TPS769 is a low-dropout (LDO) linear voltage regulator. This device supports an input voltage range from 2.5V to 16V (new chip) and up to 100mA of load current. For the new chip, the supported output range is from 1.2V to 5.0V (fixed version) or from 1.2V to 5.5V (adjustable version).

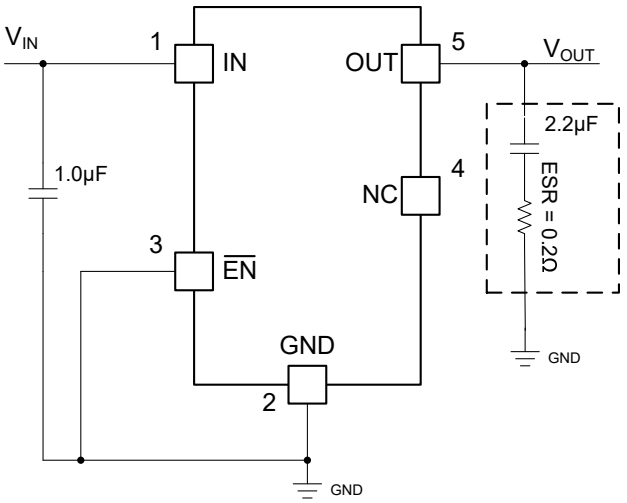
The wide input voltage range makes the device a good choice for operating from regulated rails (such as 10V or 12V). The voltage range is up to 16V for the new chip. This range allows the LDO to generate the bias voltage for a variety of applications. These applications include power microcontrollers (MCUs) and processors.

Wide bandwidth PSRR performance is greater than 70dB at 1kHz and 46dB at 1MHz (new chip). This performance helps attenuate the switching frequency of an upstream DC/DC converter and minimizes post regulator filtering. The new chip supports an internal soft-start circuit mechanism that reduces inrush current during start-up, thus allowing for smaller input capacitance.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| TPS769 | DBV (SOT-23, 5) | 2.9mm × 2.8mm |

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**Typical Application Circuit**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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# 4 Pin Configuration and Functions

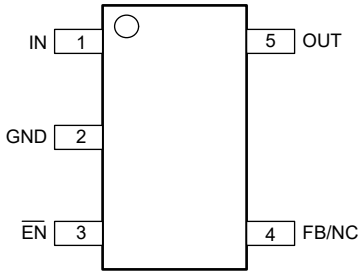


**Figure 4-1. DBV Package, 5-Pin SOT-23 (Top View)**

**Table 4-1. Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | IN | I | Input pin. Use the recommended capacitor value as listed in the *Recommended Operating Conditions* . Place the input capacitor as close to the IN and GND pins of the device as possible. See the *Input and Output Capacitor Requirements* section for more information. |
| 2 | GND | — | Ground. |
| 3 | $\overline{EN}$ | I | Enable pin. Driving the enable pin low enables the device. Driving this pin high disables the device. Low and high thresholds are listed in the *Electrical Characteristics* table. |
| 4 | FB/NC | I | Adjustable version (TPS76901-Q1): Feedback pin. Input to the control-loop error amplifier. This pin sets the output voltage of the device with external resistors. Do not float this pin. Fixed version: No connection (legacy chip). Do not connect (new chip). |
| 5 | OUT | O | Output pin. Use the recommended capacitor value as listed in the *Recommended Operating Conditions* . Place the output capacitor as close to the OUT and GND pins of the device as possible. See the *Input and Output Capacitor Requirements* section for more information. |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Continuous input voltage (legacy chip) | –0.3 | 13.5 | V |
| | Continuous input voltage (new chip) | –0.3 | 18 | |
| $V_{OUT}$ | Output voltage (legacy chip) | –0.3 | 7 | V |
| | Output voltage (new chip) | –0.3 | $V_{IN}$ + 0.3 or 7 (whichever is smaller) | |
| $V_{FB}$ | FB pin voltage (legacy chip) | –0.3 | 7 | V |
| | FB pin voltage (new chip) | –0.3 | 3 | |
| $V_{\overline{EN}}$ | $\overline{EN}$ pin voltage (legacy chip) | –0.3 | $V_{IN}$ + 0.3 | V |
| | $\overline{EN}$ pin voltage (new chip) | –0.3 | 18 | |
| Current | Maximum output | Internally limited | | A |
| Temperature | Operating junction temperature , $T_J$ (legacy chip) | –40 | 150 | °C |
| | Operating junction temperature , $T_J$ (new chip) | –55 | 150 | |
| | Storage, $T_{stg}$ | –65 | 150 | |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages with respect to GND.

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## 5.2 ESD Ratings

| | | | VALUE (Legacy Chip) | VALUE (New Chip) | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | ±3000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101(2) | N/A | ±1000 | |

(1) JEDEC document JEP155 states that 2kV HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 500V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Supply input voltage (legacy chip) | 2.7 | | 10 | V |
| | Supply input voltage (new chip) | 2.5 | | 16 | |
| $V_{OUT}$ | Output voltage (legacy chip) | 1.25 | | 5.5 | V |
| | Output voltage (new chip) | 1.2 | | 5.5 | |
| $V_{FB}$ | FB voltage (legacy chip) | | 1.224 | | V |
| | FB voltage (new chip) | | 1.2 | | |
| $V_{\overline{EN}}$ | $\overline{\text{Enable}}$ voltage (legacy chip) | 0 | | $V_{IN}$ | V |
| | $\overline{\text{Enable}}$ voltage (new chip) | 0 | | 16 | |
| $I_{OUT}$ | Output current | 0 | | 100 | mA |
| $C_{IN}$ (1) | Input capacitor | | 1 | | µF |
| $C_{OUT}$ (1) | Output capacitor (legacy chip) | 4.7 | | | µF |
| | Output capacitor (new chip) | 2.2 | | 200 | |
| ESR | ESR range (legacy chip) | 0.2 | | 10 | Ω |
| | ESR range (new chip) | 0 | | 3 | |
| $T_J$ | Operating junction temperature | –40 | | 125 | °C |

(1) All capacitor values are assumed to derate to 50% of the nominal capacitor value. Maintain an effective output capacitance of 1 µF minimum for stability.

## 5.4 Thermal Information (New Chip)

| THERMAL METRIC(1) (2) | | New Chip DBV (SOT-23-5) 5 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 178.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 77.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 47.2 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 15.9 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 46.9 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) Thermal performance results are based on the JEDEC standard of 2s2p PCB configuration. These thermal metric parameters can be further improved by 35-55% based on thermally optimized PCB layout designs. See the analysis of the Impact of board layout on LDO thermal performance application report.


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## 5.5 Thermal Information (Legacy Chip)

| DISSIPATION RATINGS | | | |
|---|---|---|---|
| THERMAL METRIC | DBV (SOT-23) 5 PINS | | UNIT |
| | Low K (1) | High K (2) | |
| $R_{\theta JC}$ (Junction-to-case thermal resistance) | 65.8 | 65.8 | °C/W |
| $R_{\theta JA}$ (Junction-to-ambient thermal resistance) | 259 | 180 | °C/W |
| Derating factor above $T_A$ = +25°C | 3.9 | 5.6 | mW/°C |
| Power rating ($T_A$ < 25°C) | 386 | 555 | mW |
| Power rating ($T_A$ = 70°C) | 212 | 305 | |
| Power rating ($T_A$ = 85°C) | 154 | 222 | |

(1) The JEDEC Low K (1s) board design used to derive this data was a 3 inch x 3 inch, two layer board with 2 ounce copper traces on top of the board.
(2) The JEDEC High K (2s2p) board design used to derive this data was a 3 inch x 3 inch, multilayer board with 1 ounce internal power and ground
planes and 2 ounce copper traces on top and bottom of the board.

## 5.6 Electrical Characteristics

specified at $T_J$ = –40°C to 125°C, $V_{IN}$ = $V_{OUT(nom)}$ + 1.0V or $V_{IN}$ = 2.5V (whichever is greater), $I_{OUT}$ = 10µA, $\overline{EN}$ = 0V, $C_{IN}$ = 1.0µF, $C_{OUT}$ = 4.7µF (unless otherwise noted); typical values are at $T_J$ = 25ºC

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OUT}$ | Output voltage | Adjustable, legacy chip | 1.2V ≤ $V_{OUT}$ ≤ 5.5V, 10µA ≤ $I_{OUT}$ ≤ 100mA, $T_J$ = 25°C | | $V_{OUT}$ | | V |
| | | | 1.2V ≤ $V_{OUT}$ ≤ 5.5V, 10µA ≤ $I_{OUT}$ ≤ 100mA | 0.97 × $V_{OUT}$ | | 1.03 × $V_{OUT}$ | |
| | | Fixed, legacy chip | 10µA ≤ $I_{OUT}$ ≤ 100mA, $T_J$ = 25°C, $V_{OUT(nom)}$ + 1V < $V_{IN}$ < 10V | | $V_{OUT}$ | | |
| | | | 10µA ≤ $I_{OUT}$ ≤ 100mA, $V_{OUT(nom)}$ + 1V < $V_{IN}$ < 10V | 0.97 × $V_{OUT}$ | | 1.03 × $V_{OUT}$ | |
| | | New chip | 10µA ≤ $I_{OUT}$ ≤ 100mA, $V_{OUT(nom)}$ + 1V < $V_{IN}$ < 16V | 0.988 × $V_{OUT}$ | | 1.012 × $V_{OUT}$ | |
| $V_{FB}$ | Feedback voltage | Legacy chip | | | 1.224 | | V |
| | | New chip | | | 1.2 | | |
| $I_Q$ | Quiescent current (GND current) | Legacy chip | $\overline{EN}$ = 0V, 0mA < $I_{OUT}$ < 100mA, $T_J$ = +25°C | | 17 | | µA |
| | | | $\overline{EN}$ = 0V, $I_{OUT}$ = 100mA | | | 28 | |
| | | New chip | $\overline{EN}$ = 0V, $I_{OUT}$ = 0mA (adjustable) | | 50 | 80 | |
| | | | $\overline{EN}$ = 0V, $I_{OUT}$ = 0mA (fixed) | | 55 | 95 | |
| | | | $\overline{EN}$ = 0V, $I_{OUT}$ = 100mA | | 620 | | |
| $\Delta V_{OUT(\Delta VOUT)}$ | Output voltage line regulation ($\Delta V_{OUT}/V_{OUT}$) | Legacy chip | $V_{OUT(NOM)}$ +1.0V ≤ $V_{IN}$ ≤ 10V, $I_{OUT}$ = 100mA, $T_J$ = 25°C | | 0.04 | 0.07 | %/V |
| | | | | | | 0.1 | |
| | | New chip | $V_{OUT(NOM)}$ +1.0V ≤ $V_{IN}$ ≤ 16V, $I_{OUT}$ = 10µA | | | 0.032 | |
| $\Delta V_{OUT(\Delta IOUT)}$ | Output voltage load regulation | Legacy chip | 0mA ≤ $I_{OUT}$ ≤ 100mA, $T_J$ = 25°C | | 12 | | mV |
| | | New chip | | | 20 | | |
| $V_n$ | Output noise voltage | Legacy chip | BW = 300Hz to 50kHz, $C_{OUT}$ = 10µF, $T_J$ = 25°C | | 190 | | $\mu V_{RMS}$ |
| | | New chip | BW = 300Hz to 50kHz, $I_{OUT}$ = 100mA, $C_{OUT}$ = 4.7µF | | 165 | | |
| | | | BW = 10Hz to 100kHz, $I_{OUT}$ = 100mA, $C_{OUT}$ = 4.7µF | | 195 | | |

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## 5.6 Electrical Characteristics (continued)

specified at $T_J$ = –40°C to 125°C, $V_{IN}$ = $V_{OUT(nom)}$ + 1.0V or $V_{IN}$ = 2.5V (whichever is greater), $I_{OUT}$ = 10µA, $\overline{EN}$ = 0V, $C_{IN}$ = 1.0µF, $C_{OUT}$ = 4.7µF (unless otherwise noted); typical values are at $T_J$ = 25ºC

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $T_{SD(shutdown)}$ | Thermal shutdown temperature | New chip | Temperature increasing | | 173 | | ºC |
| $T_{SD(reset)}$ | Thermal shutdown reset temperature | New chip | Temperature falling | | 157 | | ºC |
| $I_{CL}$ | Output current limit | Legacy chip | $V_{OUT}$ = 0V | | 350 | 750 | mA |
| | | New chip | | | 370 | 450 | |
| $I_{STANDBY}$ | Standby current | Legacy chip | $\overline{EN}$ = $V_{IN}$ , 2.7V < $V_{IN}$ < 10V | | 1 | | µA |
| | | | $\overline{EN}$ = $V_{IN}$ , 2.7V < $V_{IN}$ < 10V | | | 2 | |
| | | New chip | $\overline{EN}$ = $V_{IN}$ , 2.5V < $V_{IN}$ < 16V | | 0.9 | | |
| | | | $\overline{EN}$ = $V_{IN}$ , 2.5V < $V_{IN}$ < 16V | | | 2.75 | |
| $I_{FB}$ | Feedback pin current | Legacy chip | $V_{FB}$ = 1.224V | –1 | | 1 | µA |
| | | New chip | $V_{FB}$ = 1.2V | –0.1 | | 0.1 | µA |
| $\overline{EN}$ | High level enable input voltage | Legacy chip | 2.7V ≤ $V_{IN}$ ≤ 10V | 1.7 | | | V |
| | Low level enable input voltage | | | | | 0.9 | |
| | High level enable input voltage | New chip | 2.5V ≤ $V_{IN}$ ≤ 16V | 1.6 | | | |
| | Low level enable input voltage | | | | | 0.415 | |
| PSRR | Power-supply ripple rejection | Legacy chip | $I_{OUT}$ = 100mA, f = 1kHz, $C_{OUT}$ = 10µF, $T_J$ = 25 ℃ | | 60 | | dB |
| | | New chip | $I_{OUT}$ = 100mA, f = 1kHz, $C_{OUT}$ = 4.7µF, $T_J$ = 25℃ | | 58 | | |
| $I_{EN}$ | Input current ($\overline{EN}$) | Legacy chip | $\overline{EN}$ = 0V | –1 | 0 | 1 | µA |
| | | | $\overline{EN}$ = $V_{IN}$ | –1 | | 1 | |
| | | New chip | $\overline{EN}$ = 0V | –0.75 | –0.4 | 0.02 | |
| | | | $\overline{EN}$ = 6V | –0.01 | | 0.01 | |


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## 5.6 Electrical Characteristics (continued)

specified at $T_J$ = –40°C to 125°C, $V_{IN}$ = $V_{OUT(nom)}$ + 1.0V or $V_{IN}$ = 2.5V (whichever is greater), $I_{OUT}$ = 10µA, $\overline{EN}$ = 0V, $C_{IN}$ = 1.0µF, $C_{OUT}$ = 4.7µF (unless otherwise noted); typical values are at $T_J$ = 25ºC

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{DO}$ | Dropout voltage | TPS76928 (Legacy chip) | $I_{OUT}$ = 50mA | | 60 | | mV |
| | | | $I_{OUT}$ = 50mA, $T_J$ = –40°C to 125°C | | | 125 | |
| | | | $I_{OUT}$ = 100mA | | 122 | | |
| | | | $I_{OUT}$ = 100mA, $T_J$ = –40°C to 125°C | | | 245 | |
| | | TPS76928 (New chip) | $I_{OUT}$ = 50mA | | 120 | | |
| | | | $I_{OUT}$ = 50mA, $T_J$ = –40°C to 125°C | | | 184 | |
| | | | $I_{OUT}$ = 100mA | | 150 | | |
| | | | $I_{OUT}$ = 100mA, $T_J$ = –40°C to 125°C | | | 218 | |
| | | TPS76930 (legacy chip) | $I_{OUT}$ = 50mA | | 57 | | |
| | | | $I_{OUT}$ = 50mA, $T_J$ = –40°C to 125°C | | | 115 | |
| | | | $I_{OUT}$ = 100mA | | 115 | | |
| | | | $I_{OUT}$ = 100mA, $T_J$ = –40°C to 125°C | | | 230 | |
| | | TPS76930 (New chip) | $I_{OUT}$ = 50mA | | 120 | | |
| | | | $I_{OUT}$ = 50mA, $T_J$ = –40°C to 125°C | | | 184 | |
| | | | $I_{OUT}$ = 100mA | | 150 | | |
| | | | $I_{OUT}$ = 100mA, $T_J$ = –40°C to 125°C | | | 218 | |
| | | TPS76933 (Legacy chip) | $I_{OUT}$ = 50mA | | 48 | | |
| | | | $I_{OUT}$ = 50mA, $T_J$ = –40°C to 125°C | | | 100 | |
| | | | $I_{OUT}$ = 100mA | | 98 | | |
| | | | $I_{OUT}$ = 100mA, $T_J$ = –40°C to 125°C | | | 200 | |
| | | TPS76933 (New chip) | $I_{OUT}$ = 50mA | | 120 | | |
| | | | $I_{OUT}$ = 50mA, $T_J$ = –40°C to 125°C | | | 184 | |
| | | | $I_{OUT}$ = 100mA | | 150 | | |
| | | | $I_{OUT}$ = 100mA, $T_J$ = –40°C to 125°C | | | 218 | |
| | | TPS76950 (Legacy chip) | $I_{OUT}$ = 50mA | | 35 | | |
| | | | $I_{OUT}$ = 50mA, $T_J$ = –40°C to 125°C | | | 85 | |
| | | | $I_{OUT}$ = 100mA | | 71 | | |
| | | | $I_{OUT}$ = 100mA, $T_J$ = –40°C to 125°C | | | 170 | |
| | | TPS76950 (New chip) | $I_{OUT}$ = 50mA | | 120 | | |
| | | | $I_{OUT}$ = 50mA, $T_J$ = –40°C to 125°C | | | 184 | |
| | | | $I_{OUT}$ = 100mA | | 150 | | |
| | | | $I_{OUT}$ = 100mA, $T_J$ = –40°C to 125°C | | | 218 | |
| $V_{UVLO+}$ | Rising bias supply UVLO | TPS769 (New chip) | $V_{IN}$ rising, –40°C ≤ $T_J$ ≤ 125°C | | 2.2 | 2.4 | V |
| $V_{UVLO–}$ | Falling bias supply UVLO | | $V_{IN}$ falling, –40°C ≤ $T_J$ ≤ 125°C | 1.9 | 2.07 | | |
| $V_{UVLO(HYST)}$ | UVLO hysteresis | | –40°C ≤ $T_J$ ≤ 125°C | | 0.130 | | |

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## 5.7 Typical Characteristics

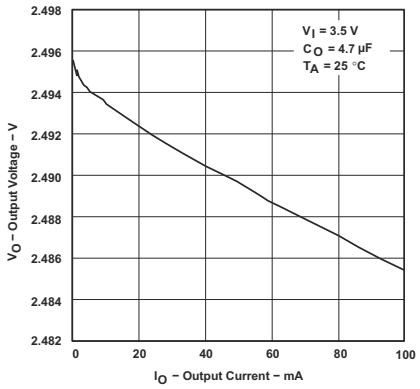


**Figure 5-1. TPS76925 Output Voltage vs Output Current (Legacy Chip)**

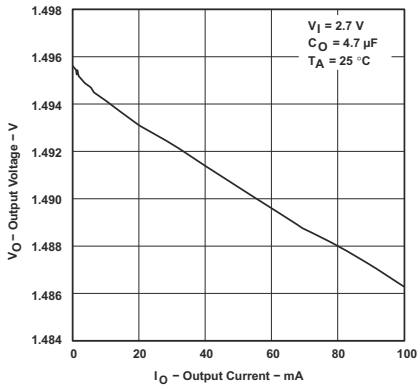


**Figure 5-2. TPS76915 Output Voltage vs Output Current (Legacy Chip)**

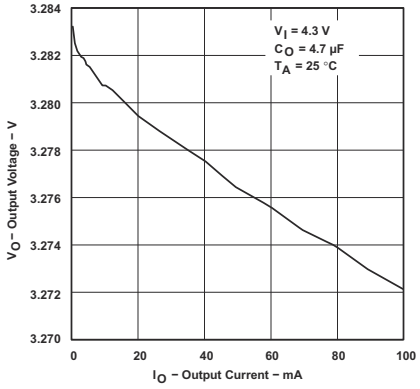


**Figure 5-3. TPS76933 Output Voltage vs Output Current (Legacy Chip)**

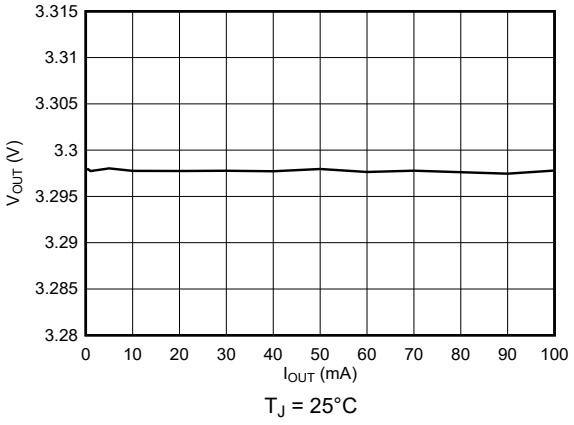


**Figure 5-4. TPS76933 Output Voltage vs Output Current (New Chip)**

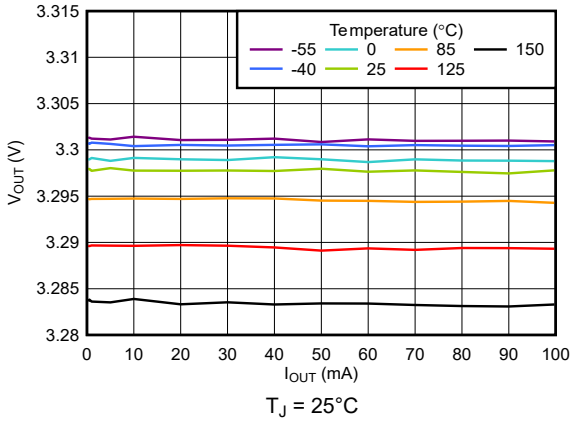


**Figure 5-5. TPS76933 Output Voltage vs Output Current (New Chip)**

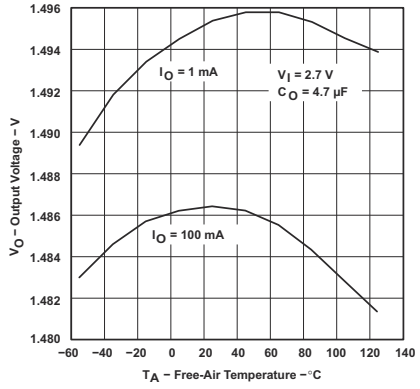


**Figure 5-6. TPS76915 Output Voltage vs Free-Air Temperature (Legacy Chip)**


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## 5.7 Typical Characteristics (continued)

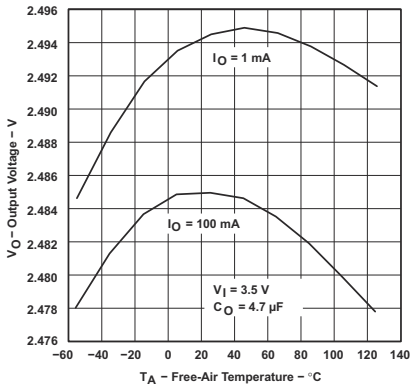


**Figure 5-7. TPS76925 Output Voltage vs Free-Air Temperature (Legacy Chip)**

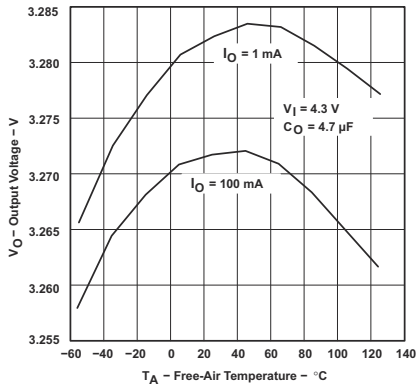


**Figure 5-8. TPS76933 Output Voltage vs Free-Air Temperature (Legacy Chip)**

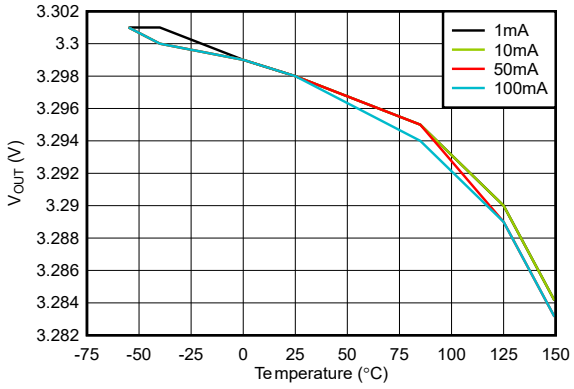


**Figure 5-9. TPS76933 Output Voltage vs Free-Air Temperature (New Chip)**

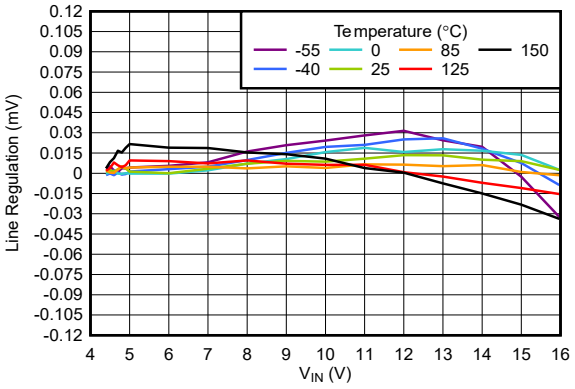


**Figure 5-10. TPS76933 Line Regulation vs Free-Air Temperature (New Chip)**

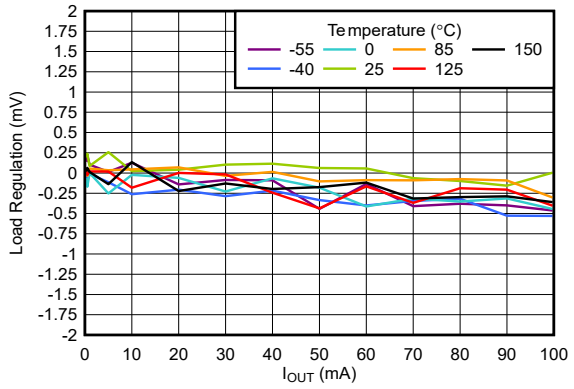


**Figure 5-11. TPS76933 Load Regulation vs Free-Air Temperature (New Chip)**

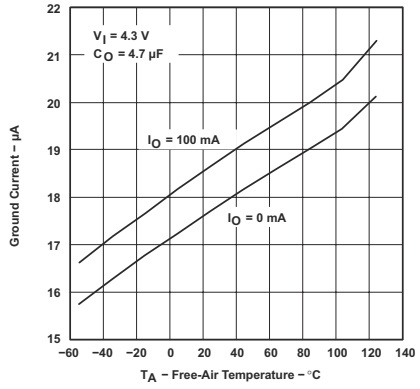


**Figure 5-12. TPS76933 Ground Current vs Free-Air Temperature (Legacy Chip)**

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## 5.7 Typical Characteristics (continued)

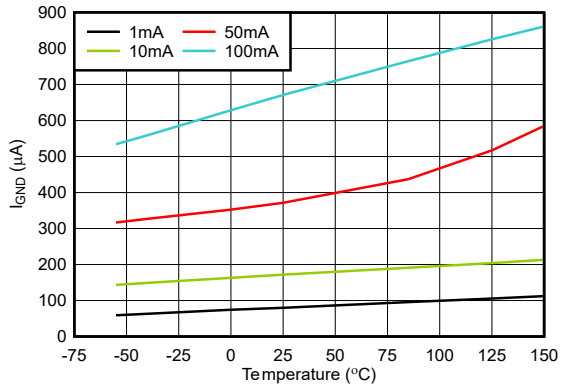


**Figure 5-13. TPS76933 Ground Current vs Free-Air Temperature (New Chip)**

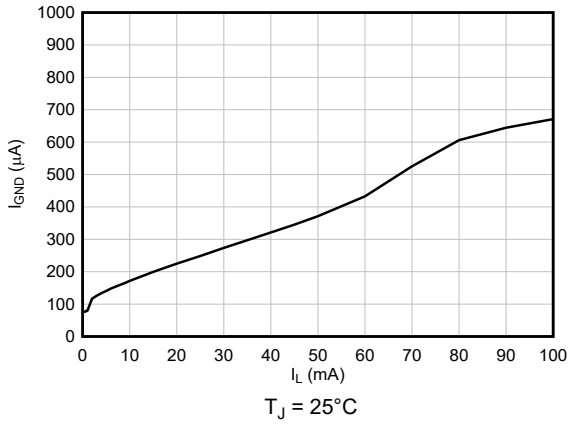


**Figure 5-14. TPS76933 Ground Current vs Output Current (New Chip)**

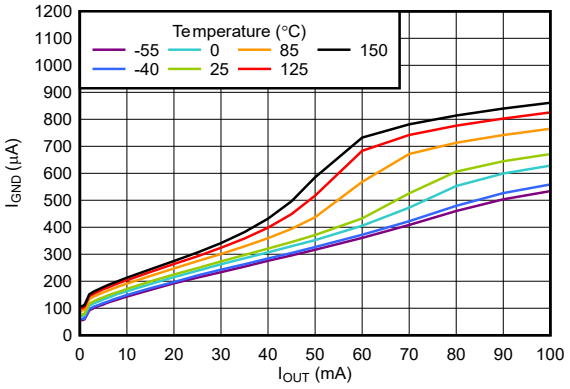


**Figure 5-15. TPS76933 Ground Current vs Output Current (New Chip)**

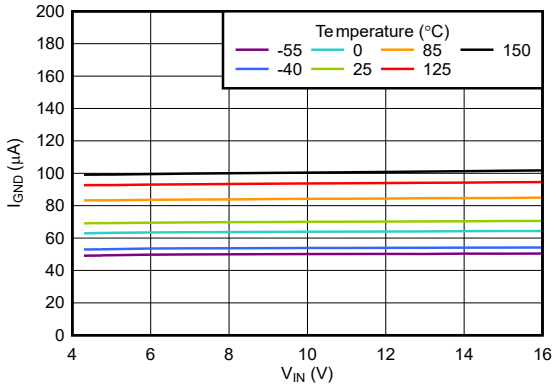


**Figure 5-16. TPS76933 Ground Current vs Input Supply (New Chip)**

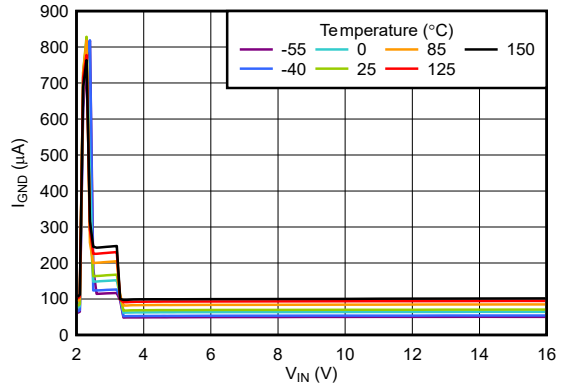


**Figure 5-17. TPS76933 Ground Current vs Input Supply (New Chip)**

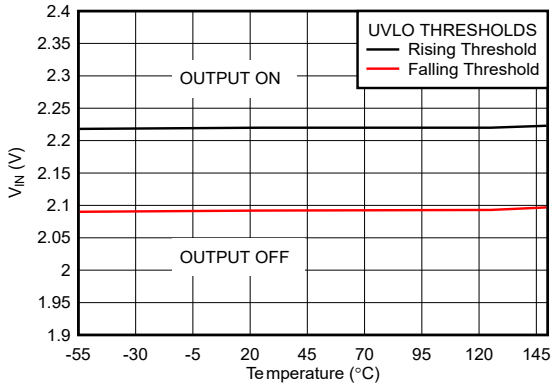


**Figure 5-18. TPS76933 UVLO Threshold vs Free-Air Temperature (New Chip)**


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## 5.7 Typical Characteristics (continued)

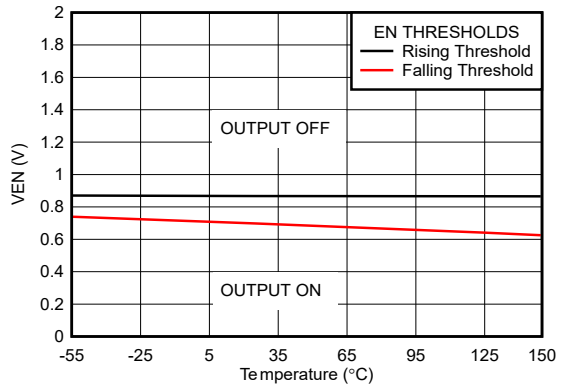



**Figure 5-19. TPS76933 EN Threshold vs Free-Air Temperature (New Chip)**

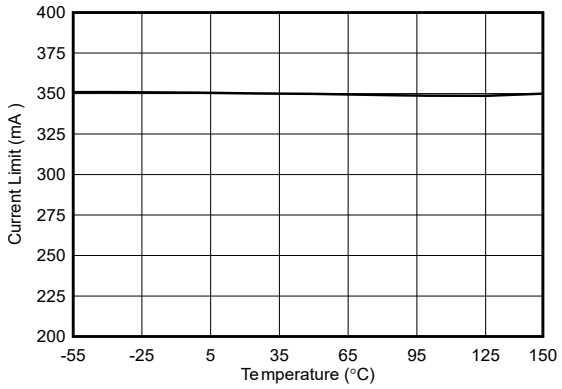



**Figure 5-20. TPS76933 Current Limit vs Free-Air Temperature (New Chip)**

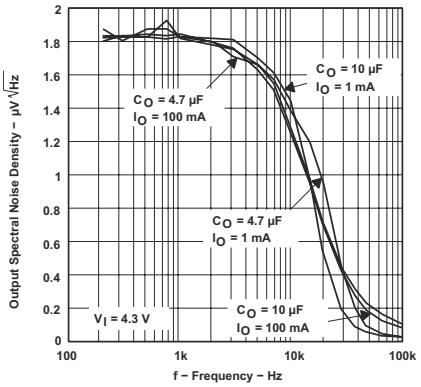



**Figure 5-21. TPS76933 Output Spectral Noise Density vs Frequency (Legacy Chip)**

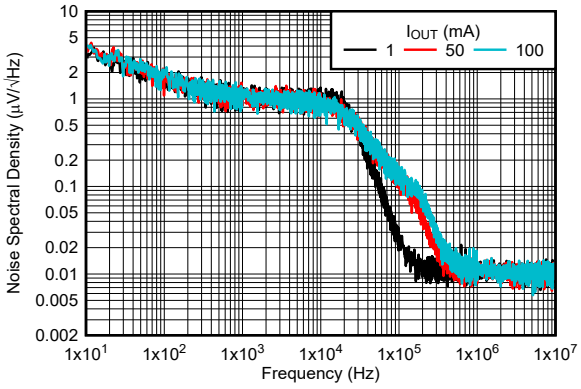



**Figure 5-22. TPS76933 Output Spectral Noise Density vs Output Current (New Chip)**

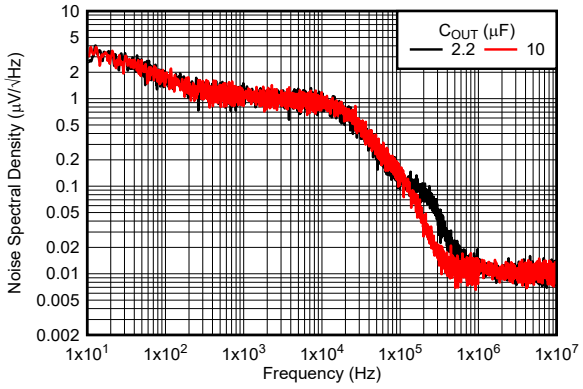
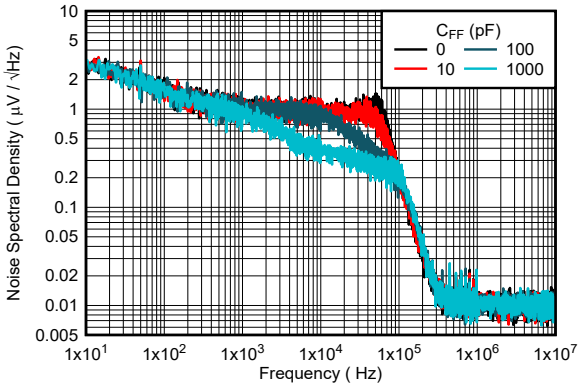



**Figure 5-23. TPS76933 Output Spectral Noise Density vs Output Capacitor (New Chip)**




IOUT = 50mA

**Figure 5-24. TPS76901 Output Spectral Noise Density vs Feed-Forward Capacitor (New Chip)**

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## 5.7 Typical Characteristics (continued)

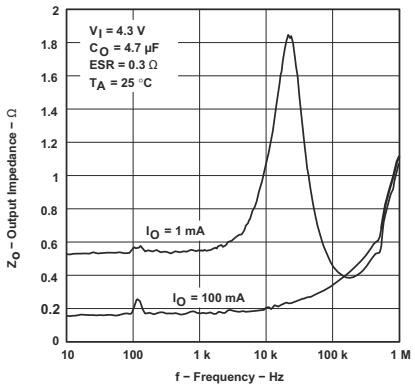


**Figure 5-25. Output Impedance vs Frequency (Legacy Chip)**

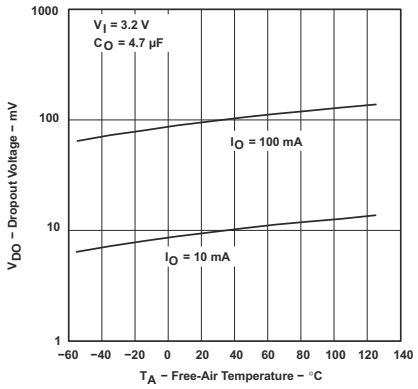


**Figure 5-26. TPS76933 Dropout Voltage vs Free-Air Temperature (Legacy Chip)**

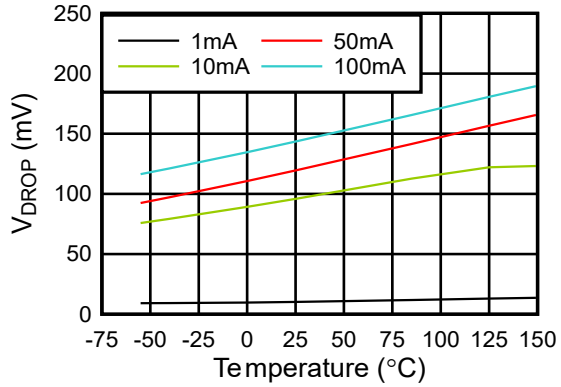


**Figure 5-27. TPS76933 Dropout Voltage vs Free-Air Temperature (New Chip)**

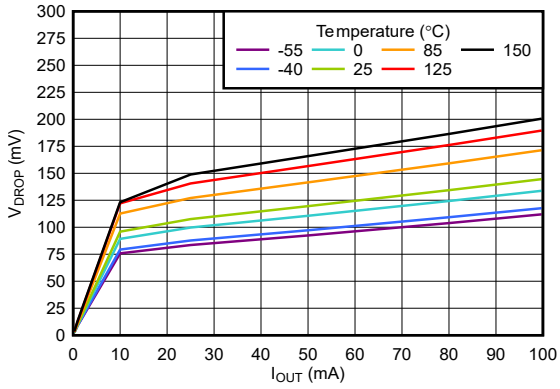


**Figure 5-28. TPS76933 Dropout Voltage vs Output Current (New Chip)**

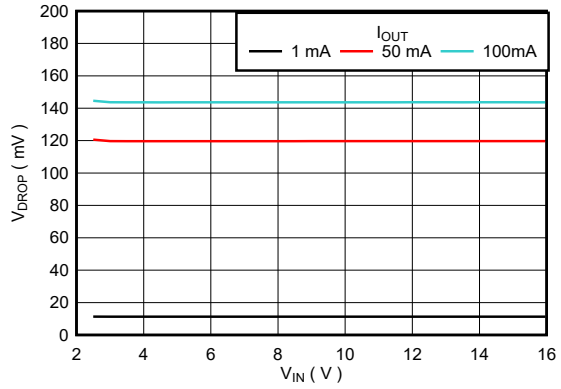


**Figure 5-29. TPS76901 Dropout Voltage vs Input Supply (New Chip)**

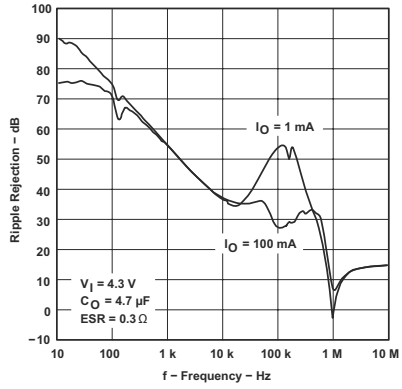


**Figure 5-30. TPS76933 Ripple Rejection vs Frequency (Legacy Chip)**


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## 5.7 Typical Characteristics (continued)

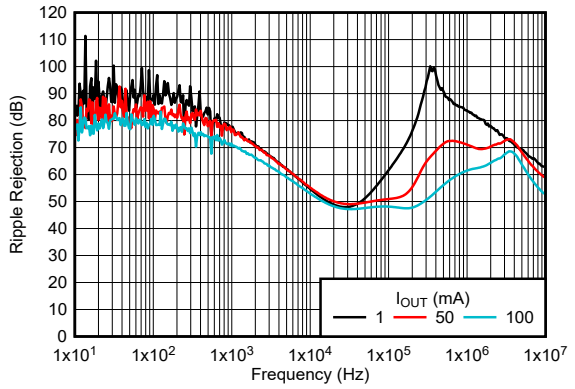
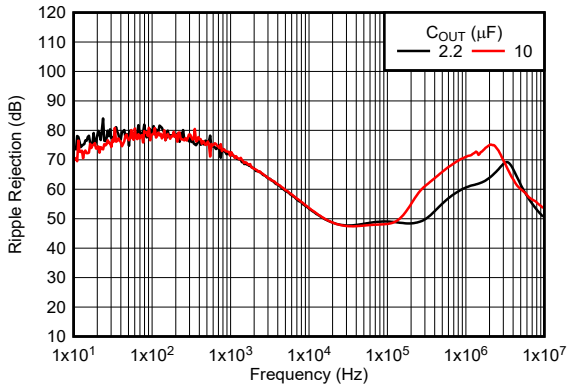
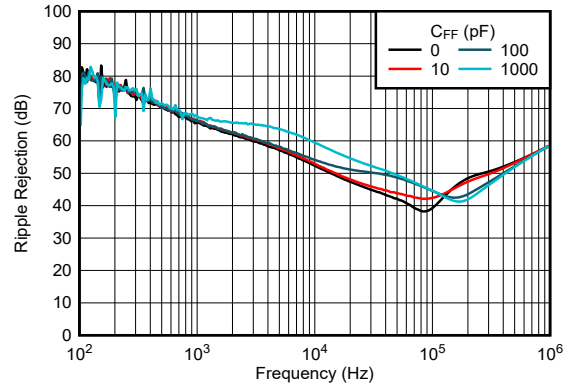



**Figure 5-31. TPS76933 Ripple Rejection vs Output Current (New Chip)**




IOUT = 100mA

**Figure 5-32. TPS76933 Ripple Rejection vs Output Capacitor (New Chip)**




IOUT = 50mA

**Figure 5-33. TPS76901 Ripple Rejection vs Feed-Forward Capacitor (New Chip)**

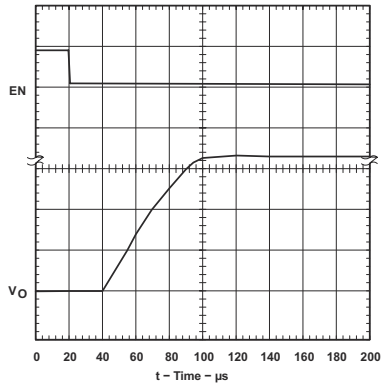



**Figure 5-34. LDO Start-Up Time (Legacy Chip)**

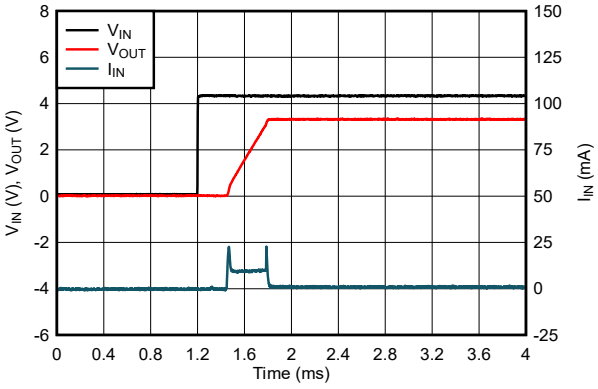



**Figure 5-35. LDO Start-Up Time With Input Supply (New Chip)**

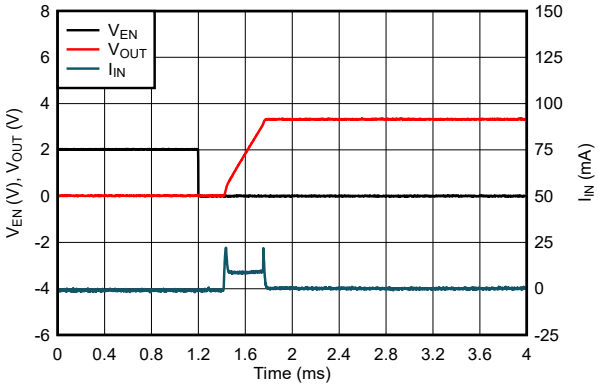



**Figure 5-36. LDO Start-Up Time With EN (New Chip)**

## 5.7 Typical Characteristics (continued)

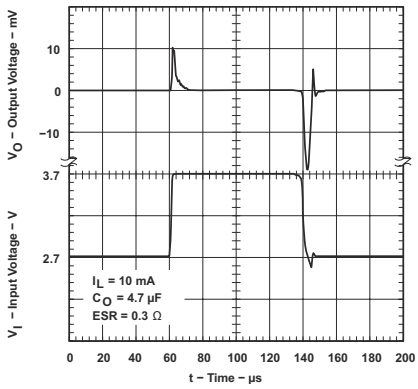



**Figure 5-37. TPS76915 Line Transient Response (Legacy Chip)**

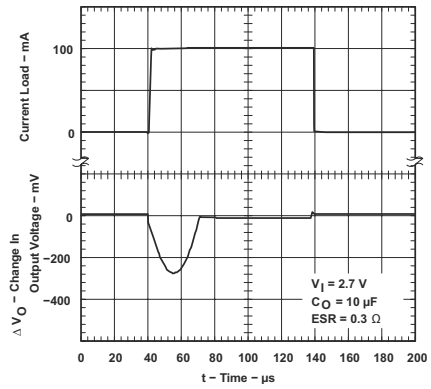



**Figure 5-38. TPS76915 Load Transient Response (Legacy Chip)**

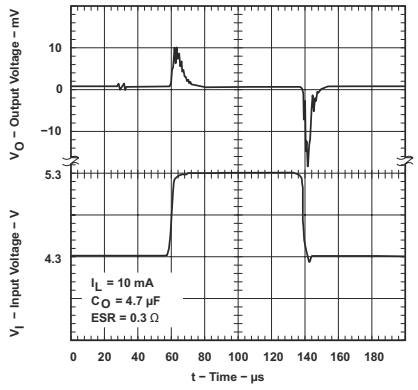
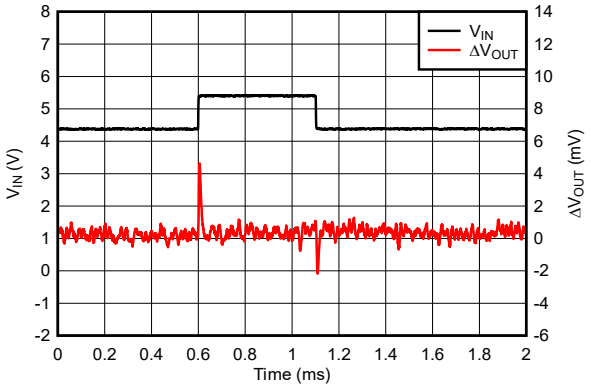
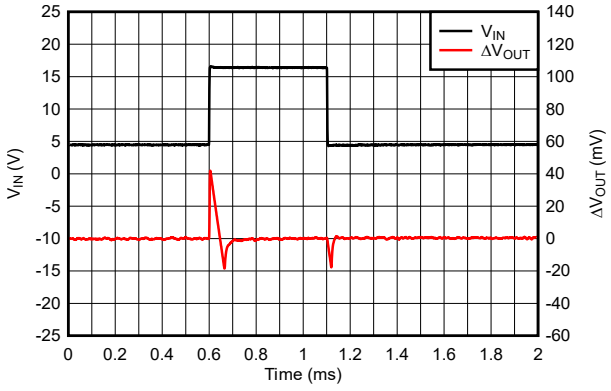



**Figure 5-39. TPS76933 Line Transient Response (Legacy Chip)**




4.3V to 5.3V at 1V/µs

**Figure 5-40. TPS76933 Line Transient Response (New Chip)**




4.3V to 16.0V at 1V/µs

**Figure 5-41. TPS76933 Line Transient Response (New Chip)**

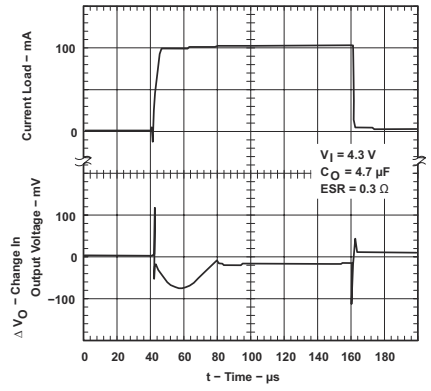



**Figure 5-42. TPS76933 Load Transient Response (Legacy Chip)**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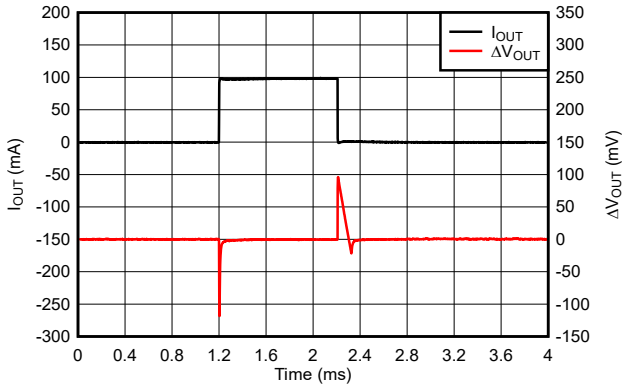
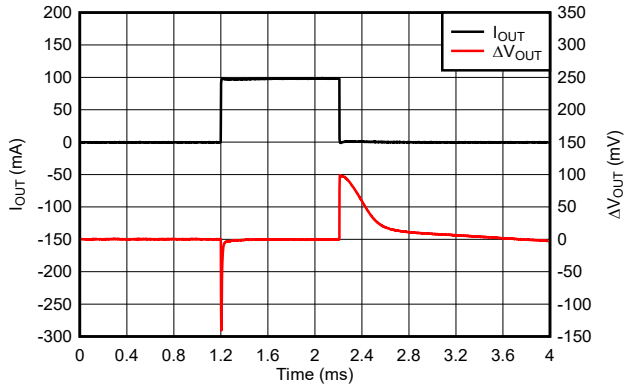
## 5.7 Typical Characteristics (continued)



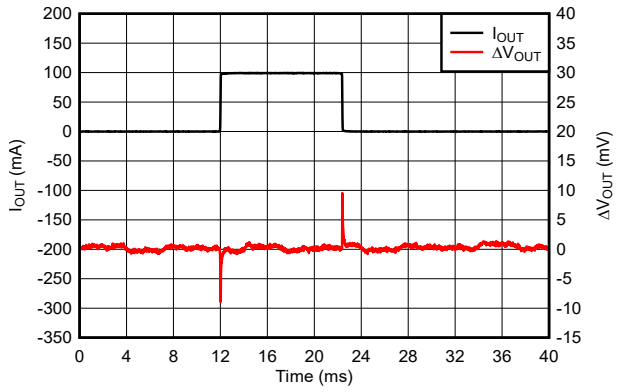

1mA to 100mA at 1A/µs

**Figure 5-43. TPS76933 Load Transient Response (New Chip)**




1µA to 100mA at 1A/µs

**Figure 5-44. TPS76933 Load Transient Response (New Chip)**




1mA to 100mA at 1mA/µs

**Figure 5-45. TPS76933 Load Transient Response (New Chip)**

## 5.8 Typical Characteristics: Supported ESR Range

Equivalent series resistance (ESR) refers to the total series resistance. This resistance includes the ESR of the capacitor, any series resistance added externally, and PCB trace resistance to $C_O$.

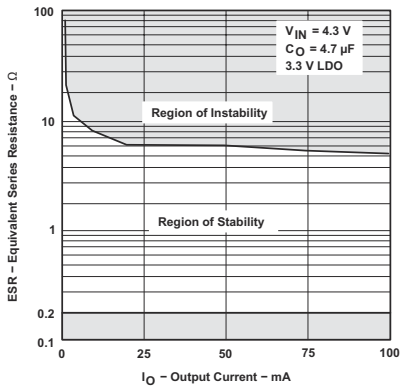



**Figure 5-46. TPS76933 Typical Regions of Stability ESR vs Output Current (Legacy Chip)**

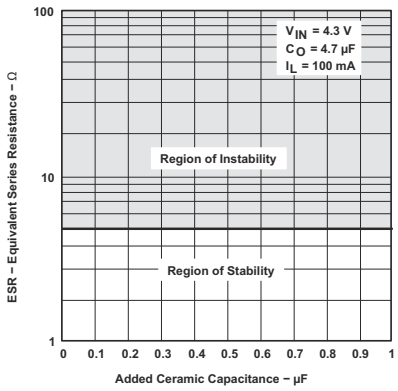



**Figure 5-47. TPS76933 Typical Regions of Stability ESR vs Added Ceramic Capacitance (Legacy Chip)**

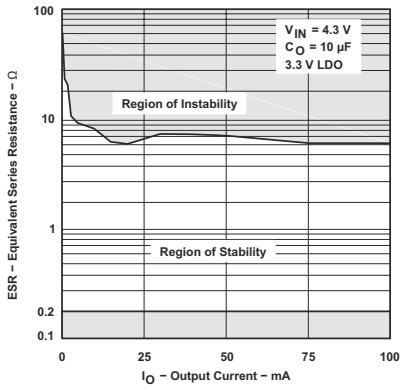



**Figure 5-48. TPS76933 Typical Regions of Stability ESR vs Output Current (Legacy Chip)**

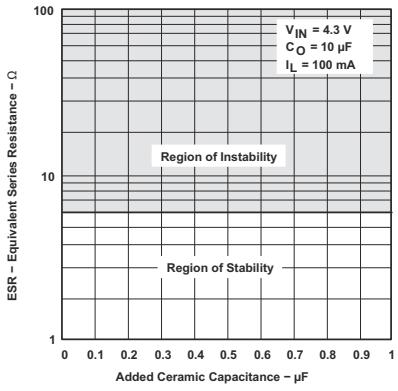



**Figure 5-49. TPS76933 Typical Regions of Stability ESR vs Added Ceramic Capacitance (Legacy Chip)**

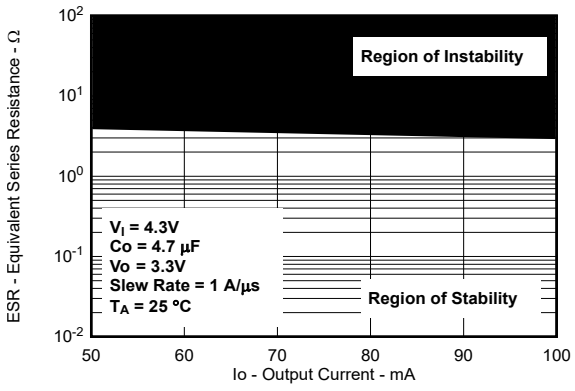



**Figure 5-50. Typical Region of Stability ESR vs Output Current (New Chip)**

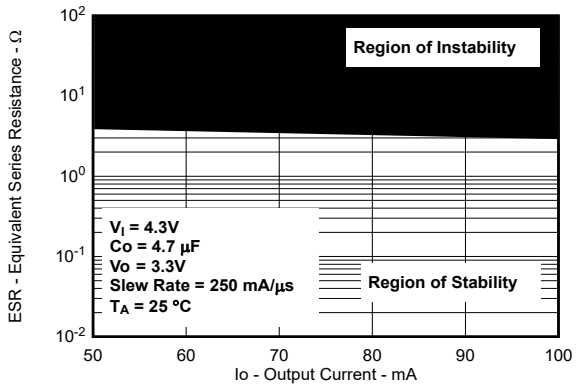



**Figure 5-51. Typical Region of Stability ESR vs Output Current (New Chip)**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## 5.8 Typical Characteristics: Supported ESR Range (continued)

Equivalent series resistance (ESR) refers to the total series resistance. This resistance includes the ESR of the capacitor, any series resistance added externally, and PCB trace resistance to $C_O$.

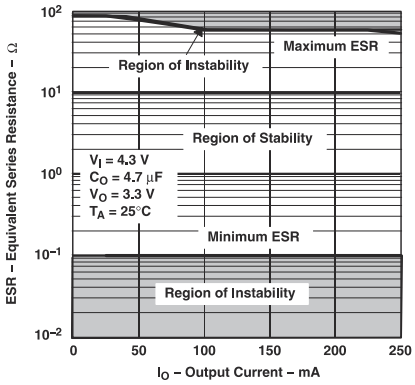


**Figure 5-52. Typical Region of Stability ESR vs Output Current (Legacy Chip)**

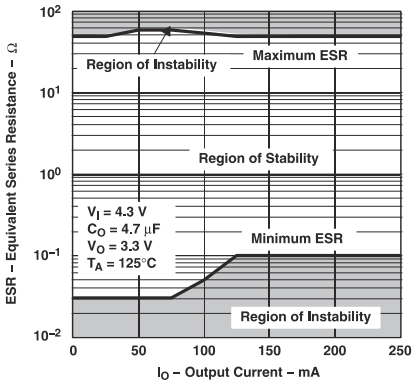


**Figure 5-53. Typical Region of Stability ESR vs Output Current (Legacy Chip)**

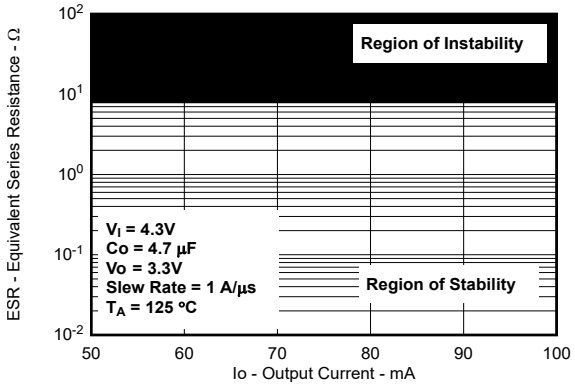


**Figure 5-54. Typical Region of Stability ESR vs Output Current (New Chip)**

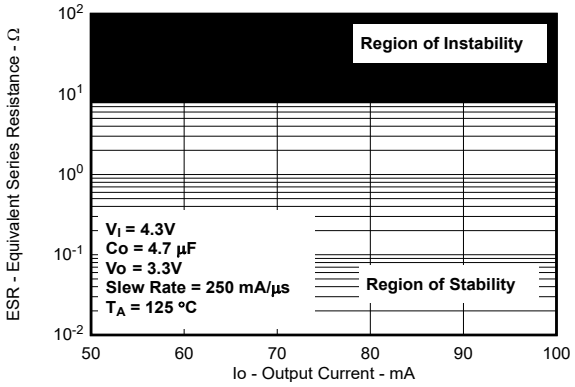


**Figure 5-55. Typical Region of Stability ESR vs Output Current (New Chip)**

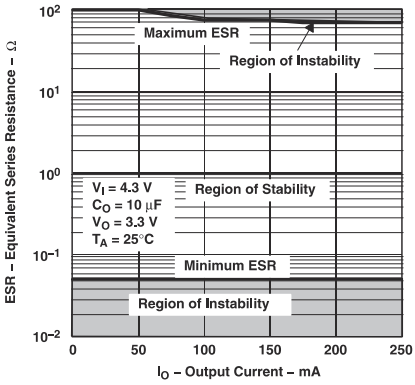


**Figure 5-56. Typical Region of Stability ESR vs Output Current (Legacy Chip)**

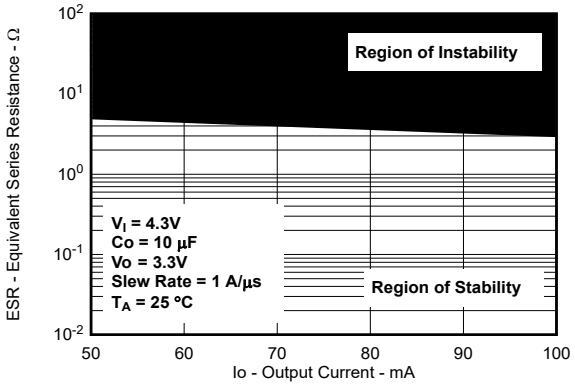


**Figure 5-57. Typical Region of Stability ESR vs Output Current (New Chip)**

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## 5.8 Typical Characteristics: Supported ESR Range (continued)

Equivalent series resistance (ESR) refers to the total series resistance. This resistance includes the ESR of the capacitor, any series resistance added externally, and PCB trace resistance to $C_O$.

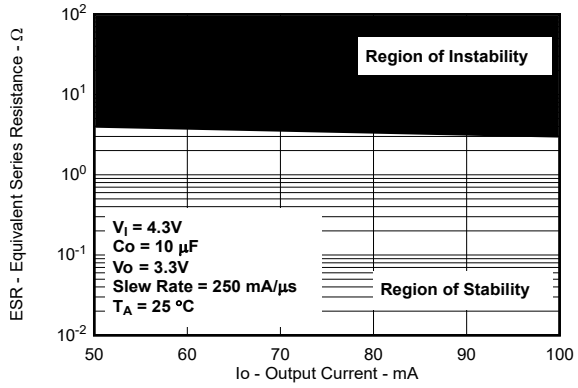


**Figure 5-58. Typical Region of Stability ESR vs Output Current (New Chip)**

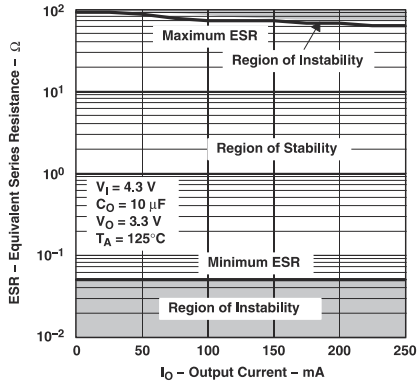


**Figure 5-59. Typical Region of Stability ESR vs Output Current (Legacy Chip)**

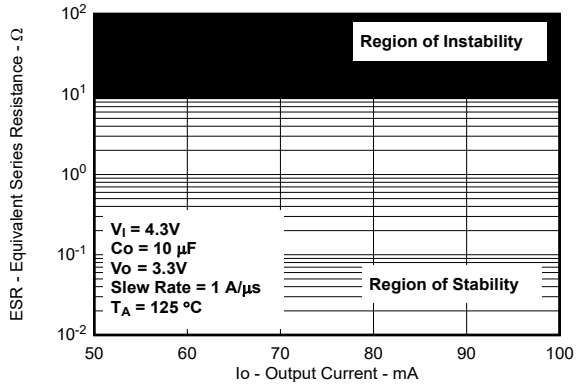


**Figure 5-60. Typical Region of Stability ESR vs Output Current (New Chip)**

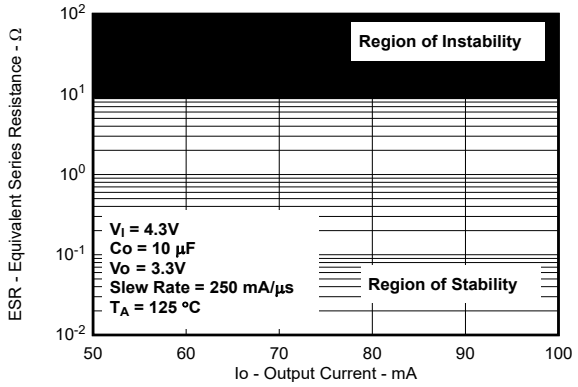


**Figure 5-61. Typical Region of Stability ESR vs Output Current (New Chip)**

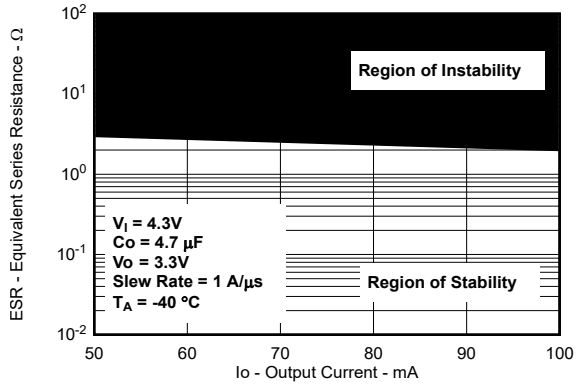


**Figure 5-62. Typical Region of Stability ESR vs Output Current (New Chip)**

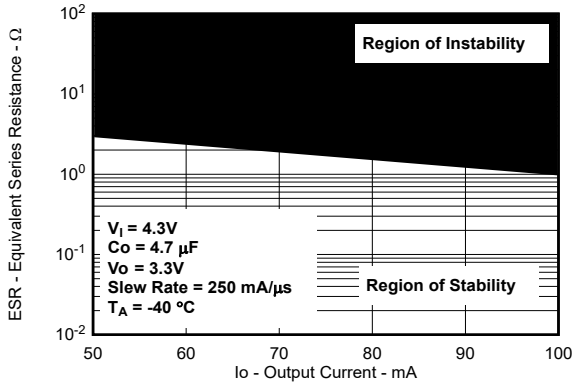


**Figure 5-63. Typical Region of Stability ESR vs Output Current (Legacy Chip)**


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## 5.8 Typical Characteristics: Supported ESR Range (continued)

Equivalent series resistance (ESR) refers to the total series resistance. This resistance includes the ESR of the capacitor, any series resistance added externally, and PCB trace resistance to $C_O$.

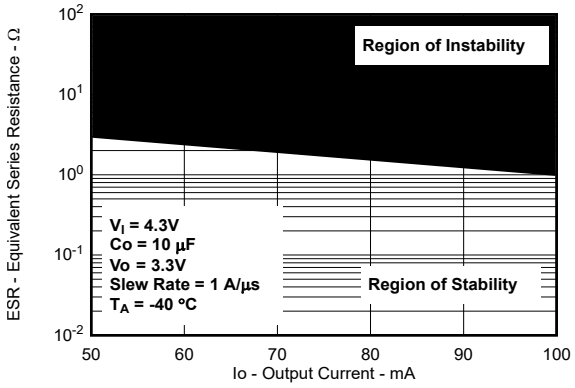


**Figure 5-64. Typical Region of Stability ESR vs Output Current (New Chip)**

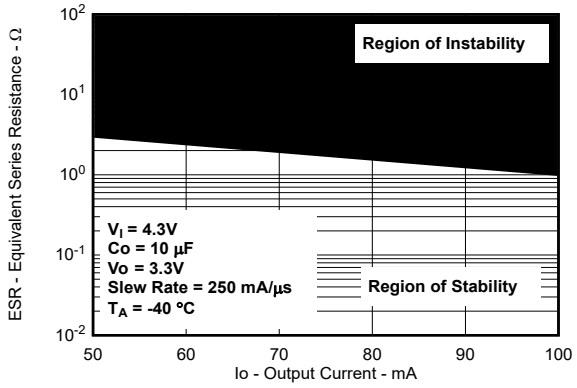


**Figure 5-65. Typical Region of Stability ESR vs Output Current (New Chip)**

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# 6 Detailed Description

## 6.1 Overview

The TPS769 is a low quiescent current, high PSRR, low-dropout (LDO) voltage regulator capable of handling up to 100mA of load current. The TPS769 is optimized for use in battery-powered and automotive applications.

The TPS769 features an integrated overcurrent limit, thermal shutdown, output enable, internal output pulldown, and undervoltage lockout (UVLO for the new chip). This device delivers excellent line and load transient performance and supports a wide range of ESR (up to 2Ω for the new chip). The operating ambient temperature range of the device is –40°C to +125°C.

## 6.2 Functional Block Diagrams

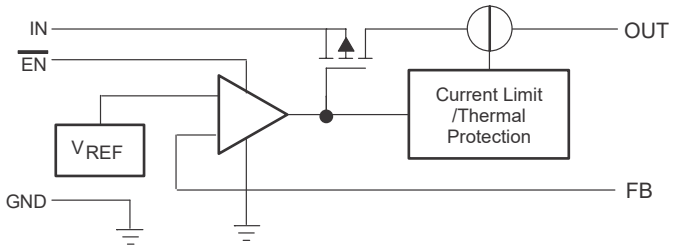


**Figure 6-1. TPS76901 Functional Block Diagram (Legacy Chip)**

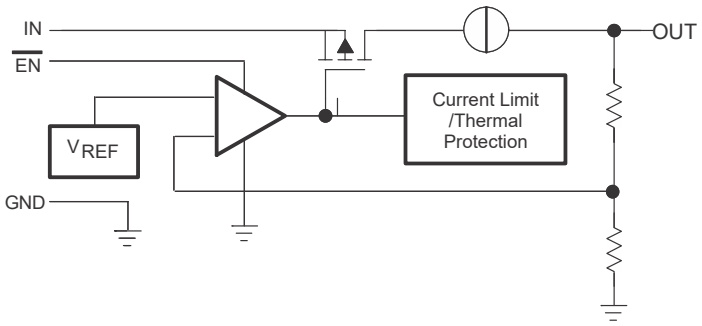


**Figure 6-2. TPS769 Functional Block Diagram (Legacy Chip)**

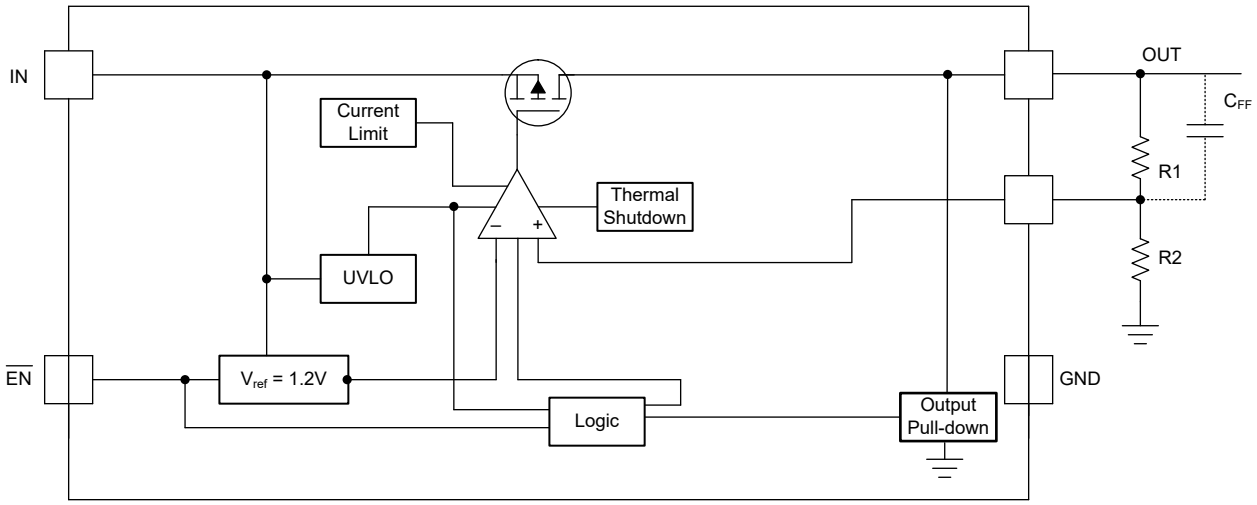


**Figure 6-3. TPS76901 Adjustable Functional Block Diagram (New Chip)**


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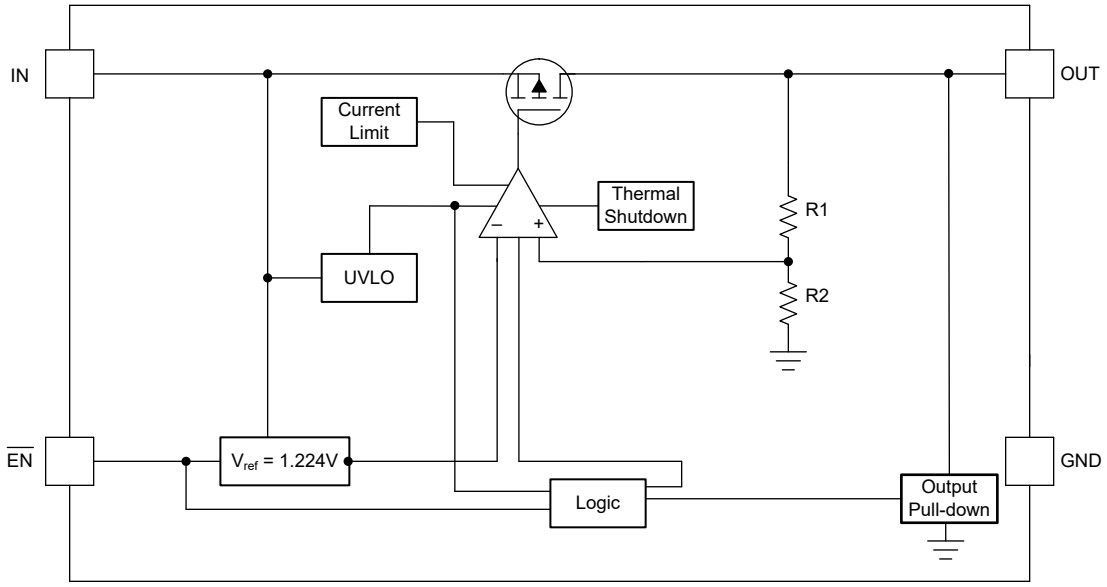


**Figure 6-4. TPS769 Fixed Functional Block Diagram (New Chip)**

## 6.3 Feature Description

### *6.3.1 Output Enable*

The enable pin for the device is an active-low pin. The output voltage is enabled when the voltage of the enable pin is lower than the low-level input voltage of the $\overline{EN}$ pin. The output voltage is disabled when the enable pin voltage is higher than the high-level input voltage of the $\overline{EN}$ pin. If $\overline{EN}$ functionality is not needed, connect the enable pin to the GND of the device.

For the new chip, there is an internal pullup current on the $\overline{EN}$ pin. Therefore, leave the $\overline{EN}$ pin floating. If the $\overline{EN}$ pin is left floating, the LDO is disabled.

In the new chip, the device has an internal output pulldown circuit that activates when the device is disabled to actively discharge the output voltage. See the *Output Pulldown* section for further information.

### *6.3.2 Dropout Voltage*

Dropout voltage ($V_{DO}$) is defined as $V_{IN} - V_{OUT}$ at the rated output current ($I_{RATED}$), where the pass transistor is fully on. $V_{IN}$ is the input voltage, $V_{OUT}$ is the output voltage, and $I_{RATED}$ is the maximum $I_{OUT}$ listed in the *Recommended Operating Conditions* table. At this operating point, the pass transistor is driven fully on. Dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage where the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source, on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

### *6.3.3 Current Limit*

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brick-wall scheme. In a high-load current fault, the brick-wall scheme limits the output current to the current limit ($I_{CL}$). $I_{CL}$ is listed in the *Electrical Characteristics* table.

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The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [($V_{IN}$ – $V_{OUT}$) × $I_{CL}$]. For more information on current limits, see the *Know Your Limits* application note.

Figure 6-5 shows a diagram of the current limit.

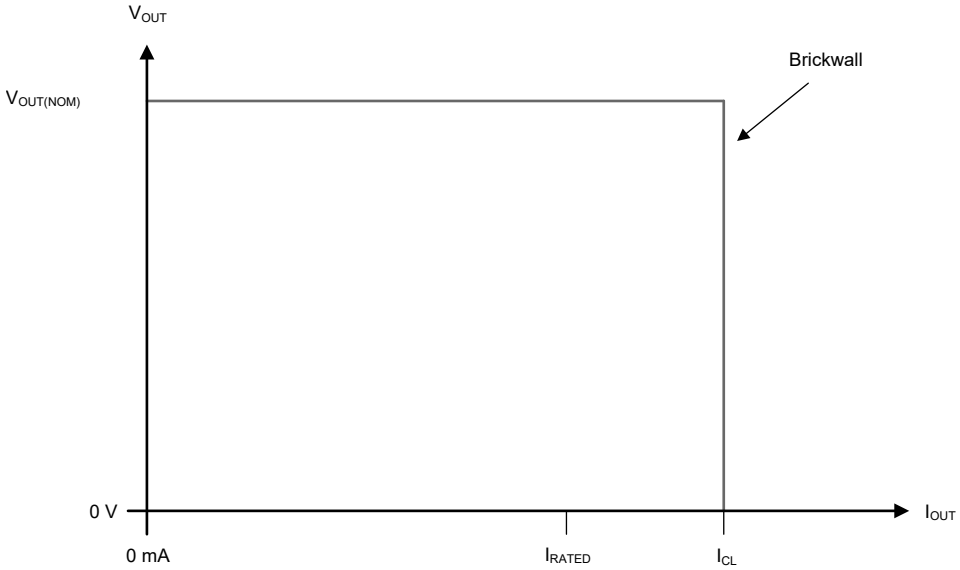


**Figure 6-5. Current Limit**

### *6.3.4 Undervoltage Lockout (UVLO)*

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage. Thus, allowing a controlled and consistent turn on and off of the output voltage. The UVLO circuit has hysteresis functionality to prevent the device from turning off if the input drops during turn on.

### *6.3.5 Output Pulldown*

The device (new chip) has an output pulldown circuit. The output pulldown circuit activates under the following conditions:

- The device is disabled with $\overline{EN}$ logic
- 1.0V < $V_{IN}$ < $V_{UVLO}$

The output pulldown resistance for this device is 1.5kΩ (typ), as listed in the *Electrical Characteristics* table.

Reverse current flows from the output to the input. Thus, do not rely on the output pulldown circuit for discharging a large amount of output capacitance after the input supply collapses. This reverse current flow potentially causes damage to the device. See the *Reverse Current* section for more details.


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### 6.3.6 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature ($T_J$) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis makes sure that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short. Thus the device cycles on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start-up is high from large $V_{IN} – V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start-up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the device internal protection circuitry is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

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## 6.4 Device Functional Modes

Table 6-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

**Table 6-1. Device Functional Mode Comparison**

| OPERATING MODE | PARAMETER | | | |
|---|---|---|---|---|
| | $V_{IN}$ | $V_{EN}$ | $I_{OUT}$ | $T_J$ |
| Normal operation | $V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$ | $V_{EN} < V_{EN(LOW)}$ | $I_{OUT} < I_{OUT(max)}$ | $T_J < T_{SD(shutdown)}$ |
| Dropout operation | $V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$ | $V_{EN} < V_{EN(LOW)}$ | $I_{OUT} < I_{OUT(max)}$ | $T_J < T_{SD(shutdown)}$ |
| Disabled (any true condition disables the device) | $V_{IN} < V_{UVLO}$ | $V_{EN} > V_{EN(HI)}$ | Not applicable | $T_J > T_{SD(shutdown)}$ |

### *6.4.1 Normal Operation*

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$).
- The current sourced from OUT is less than the current limit ($I_{OUT} < I_{CL(OUT)}$).
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$).
- The enable voltage has previously receded the enable low level threshold voltage and has not yet increased higher than the enable high level threshold. Or the $\overline{EN}$ pin is connected to ground.

### *6.4.2 Dropout Operation*

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. In this mode, the transient performance of the device becomes significantly degraded. During this mode, the pass transistor is driven fully on. Line or load transients in dropout potentially result in large output voltage deviations.

When the device is in a steady dropout state, the pass transistor is driven fully on. This state is defined as when the device is in dropout, directly after being in a normal regulation state, but *not* during start-up. Dropout occurs when $V_{IN} < V_{OUT(NOM)} + V_{DO}$. When the regulator exits dropout, the input voltage returns to a value $\geq V_{OUT(NOM)} + V_{DO}$. During this time, the output voltage potentially overshoots for a short period of time. $V_{OUT(NOM)}$ is the nominal output voltage and $V_{DO}$ is the dropout voltage. During dropout exit, the device pulls the pass transistor back from being driven fully on.

### *6.4.3 Disabled*

Shutdown the device output by forcing the enable pin voltage to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor turns off and internal circuits shut down. The output voltage is also actively discharged to ground by an internal discharge circuit from the output to ground.


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# 7 Application and Implementation

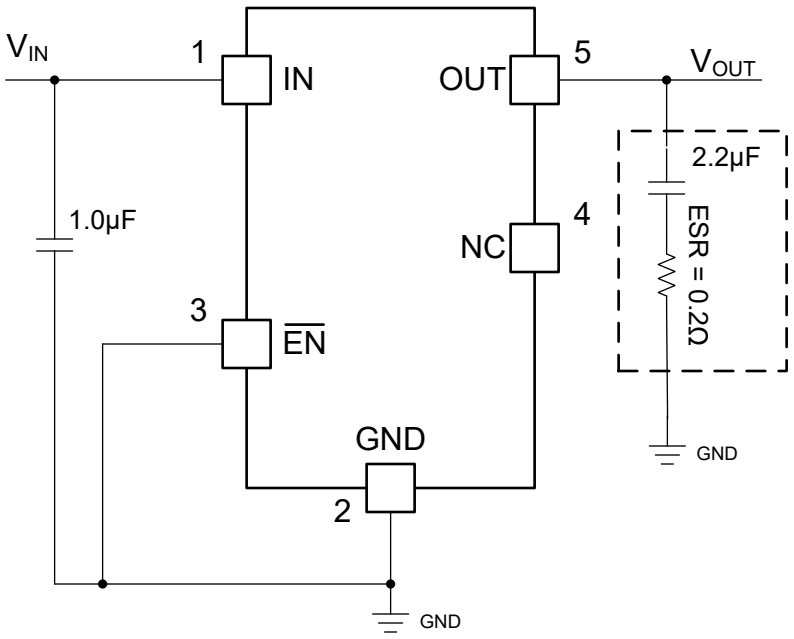
**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 7.1 Application Information

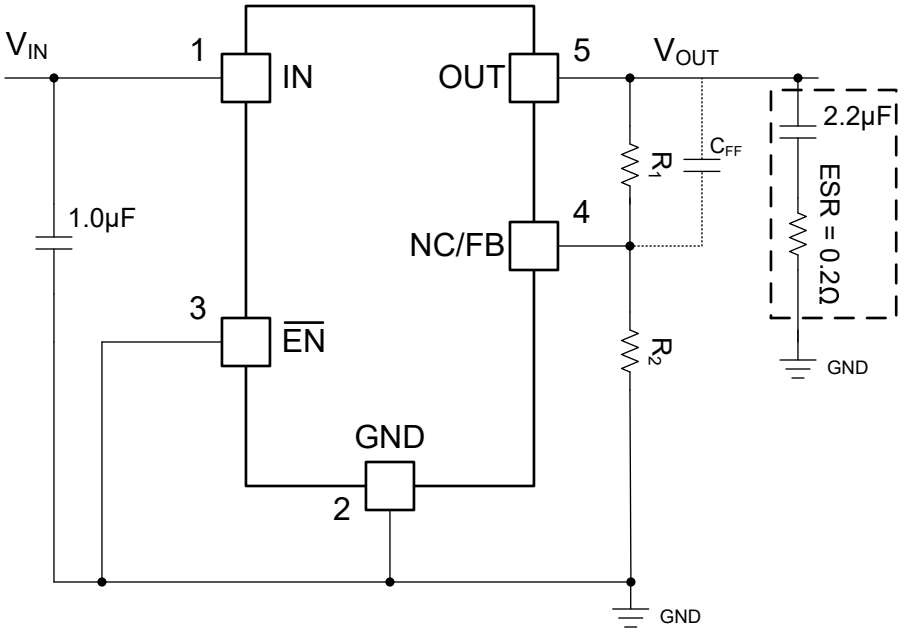
The TPS769 low-dropout (LDO) regulator is optimized for use in battery-operated equipment. This device features extremely low dropout voltages, low quiescent current (55µA nominally, for the new chip), and enable inputs. The enable inputs reduce supply currents to 1µA when the regulators are turned off.

## 7.2 Typical Application




For fixed output voltage options only.

**Figure 7-1. Typical Application Circuit (Fixed-Voltage Option)**




For adjustable output voltage options only. Dotted lines indicate an optional $C_{FF}$ capacitor (new chip). See the *Feed-Forward Capacitor ($C_{FF}$)* section.

**Figure 7-2. Typical Application Circuit (Adjustable-Voltage Option)**

Table 7-1 lists the $R_1$ and $R_2$ resistor values for the adjustable-voltage version.

**Table 7-1. Adjustable Output Voltage for Resistors $R_1$ and $R_2$**

| OUTPUT VOLTAGE | $R_1$ (kΩ) | $R_2$ (kΩ) |
|---|---|---|
| 2.5V | 174 | 169 |
| 3.3V | 287 | 169 |
| 3.6V | 324 | 169 |
| 4.0V | 383 | 169 |
| 5.0V | 523 | 169 |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### 7.2.1 Design Requirements

Table 7-2 lists the design parameters for this example.

**Table 7-2. Design Parameters**

| PARAMETER | EXAMPLE VALUE |
|---|---|
| Input voltage range | 4V to 10V |
| Output voltage | 2.5V to 5V |
| Output current rating | 100mA |
| Output capacitor | 4.7µF to 10µF |
| Output capacitor ESR range | 200mΩ to 2Ω |

### 7.2.2 Detailed Design Procedure

#### 7.2.2.1 Adjustable Device Feedback Resistors

The adjustable-version device requires external feedback divider resistors to set the output voltage. $V_{OUT}$ is set using the feedback divider resistors, $R_1$ and $R_2$, according to the following equation:

$$V_{OUT} = V_{REF} \times (1 + R_1 / R_2) \quad (2)$$

where:

- $V_{REF}$ = 1.205V (typ) for the internal reference voltage (for the new chip)

To ignore the FB pin current error term in the $V_{OUT}$ equation, set the feedback divider current to 100 times the FB pin current. This current is listed in the *Electrical Characteristics* table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \leq V_{OUT} / (I_{FB} \times 100) \quad (3)$$

In Table 7-1, examples of $R_1$ and $R_2$ values are given for different output voltage options with a feedback divider current designed at 7µA.

#### 7.2.2.2 Recommended Capacitor Types

The device (new chip) is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but use good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature. However, using Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors listed in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

#### 7.2.2.3 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5Ω. Use a higher value capacitor if large, fast rise-time, load, or line transients are anticipated. Additionally, use a higher-value capacitor if the device is located several inches from the input power source.

As with most low-dropout regulators, the TPS769 requires an output capacitor connected between OUT and GND to stabilize the internal control loop.

For the legacy chip, the device requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 4.7µF. Make sure the equivalent series resistance (ESR) of the capacitor is between 0.2Ω and 10Ω to provide stability. Capacitor values larger than 4.7µF are acceptable, and allow the use of smaller ESR values. Capacitances less than 4.7µF are not

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recommended because these components require careful selection of ESR to provide stability. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided these capacitors meet the described requirements. Most of the commercially available 4.7µF surface-mount solid tantalum capacitors, including devices from Sprague, Kemet, and Nichico, meet the ESR requirements previously stated. Multilayer ceramic capacitors potentially have very small equivalent series resistances and therefore require the addition of a low value series resistor to provide stability.

For the new chip, the device is designed to be stable using low ESR ceramic capacitors at the input and output. The minimum recommended capacitance value is 2.2µF and the ESR range is up to 2Ω. The supported ESR range depends on the output capacitance, operating junction temperature, and load current conditions. The *Typical Characteristics: Supported ESR Range* describes the supported ESR range in regards to the output capacitance across temperature for the supported load current range.

Dynamic performance of the device is improved by using an output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

#### 7.2.2.4 Reverse Current

Excessive reverse current potentially damages this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current occur are outlined in this section, all of which potentially exceed the absolute maximum rating of $V_{OUT} \leq V_{IN} + 0.3V$.

- If the device has a large $C_{OUT}$ and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, use external protection to protect the device. Reverse current is not limited in the device, so use external limiting if extended reverse voltage operation is anticipated.

Figure 7-3 shows one approach for protecting the device.

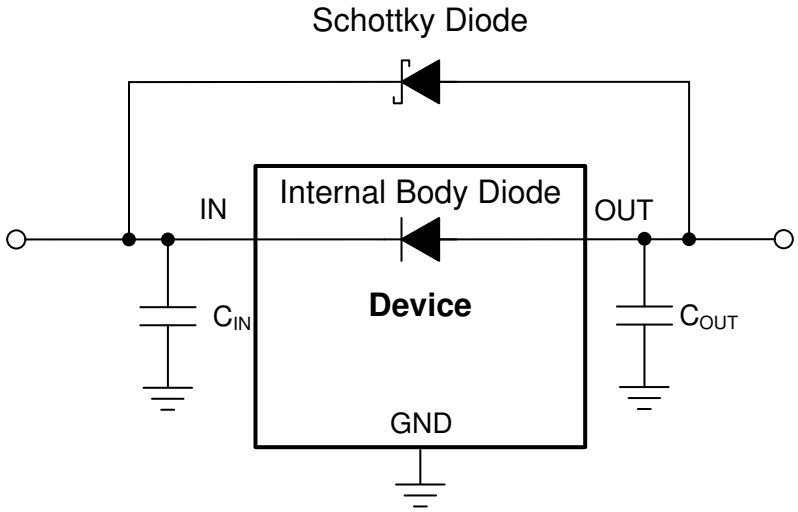


**Figure 7-3. Example Circuit for Reverse Current Protection Using a Schottky Diode**

#### 7.2.2.5 Feed-Forward Capacitor ($C_{FF}$)

For the adjustable-voltage version device, connect a feed-forward capacitor ($C_{FF}$) from the OUT pin to the FB pin. $C_{FF}$ improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended $C_{FF}$ values are listed in the *Recommended Operating Conditions* table. If a higher capacitance $C_{FF}$ is used, the start-up time increases. For a detailed description of $C_{FF}$ tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note.


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$C_{FF}$ and $R_1$ form a zero in the loop gain at frequency $f_Z$. $C_{FF}$, $R_1$, and $R_2$ form a pole in the loop gain at frequency $f_P$. Calculate the $C_{FF}$ zero and pole frequencies from the following equations:

$$f_Z = 1 / (2 \times \pi \times C_{FF} \times R_1) \quad (4)$$

$$f_P = 1 / (2 \times \pi \times C_{FF} \times (R_1 \parallel R_2)) \quad (5)$$

$C_{FF} \geq 10pF$ is required for stability if the feedback divider current is less than 5µA. The following equation calculates the feedback divider current.

$$I_{FB_Divider} = V_{OUT} / (R_1 + R_2) \quad (6)$$

To avoid start-up time increases from $C_{FF}$, limit the product $C_{FF} \times R_1$ to less than 50µs.

For an output voltage of 1.2V (for new chip) with the FB pin tied to the OUT pin, no $C_{FF}$ is used.

#### 7.2.2.6 Power Dissipation ($P_D$)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct thermal plane sizing. Place few or no other heat-generating devices that cause added thermal stress in the PCB area around the regulator.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation ($P_D$).

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (7)$$

**Note**

Minimize power dissipation, and therefore achieve greater efficiency, by correctly selecting the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature ($T_A$) for the device. Power dissipation and junction temperature are most often related by the $R_{\theta JA}$ of the combined PCB, device package, and the ambient air temperature ($T_A$). $R_{\theta JA}$ is the junction-to-ambient thermal resistance. The following equation calculates this relationship.

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (8)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design. $R_{\theta JA}$ therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information (New Chip)* table is determined by the JEDEC standard PCB and copper-spreading area. $R_{\theta JA}$ is used as a relative measure of package thermal performance. $R_{\theta JA}$ is improved by 35% to 55% compared to the *Thermal Information (New Chip)* table value by optimizing the PCB board layout. See the *An empirical analysis of the impact of board layout on LDO thermal performance* application note for further information.

#### 7.2.2.7 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics. These metrics estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat spreading. The *Thermal Information (New Chip)* table lists the primary thermal metrics, which are the junction-to-top

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characterization parameter ($\psi_{JT}$) and junction-to-board characterization parameter ($\psi_{JB}$). These parameters provide two methods for calculating the junction temperature ($T_J$), as described in the following equations. Use the junction-to-top characterization parameter ($\psi_{JT}$) with the temperature at the center-top of device package ($T_T$) to calculate the junction temperature. Use the junction-to-board characterization parameter ($\psi_{JB}$) with the PCB surface temperature 1mm from the device package ($T_B$) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \quad (9)$$

where:

- $P_D$ is the dissipated power
- $T_T$ is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \quad (10)$$

where:

- $T_B$ is the PCB surface temperature measured 1mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.


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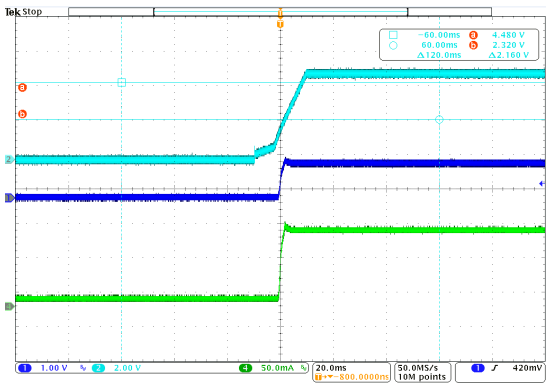
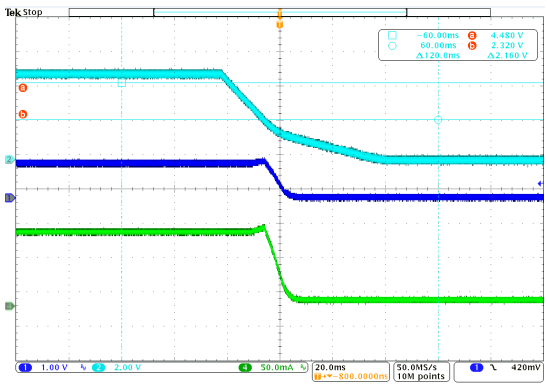
### 7.2.3 Application Curves




Channel 1 = $V_{OUT}$, channel 2 = $V_{IN}$, channel 4 = $I_{OUT}$

**Figure 7-4. Power-Up Waveform (Legacy Chip)**




Channel 1 = $V_{OUT}$, channel 2 = $V_{IN}$, channel 4 = $I_{OUT}$

**Figure 7-5. Pow**

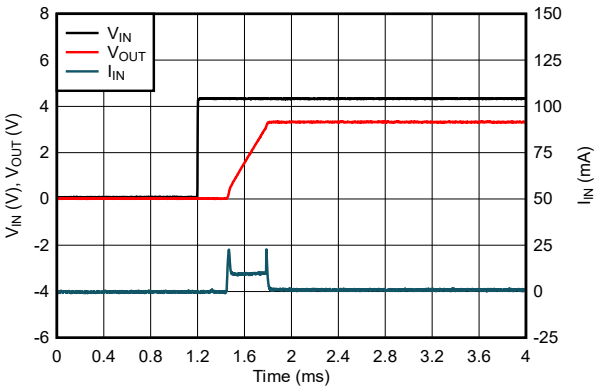



**Figure 7-6. LDO Start-Up Time With Input supply (New Chip)**

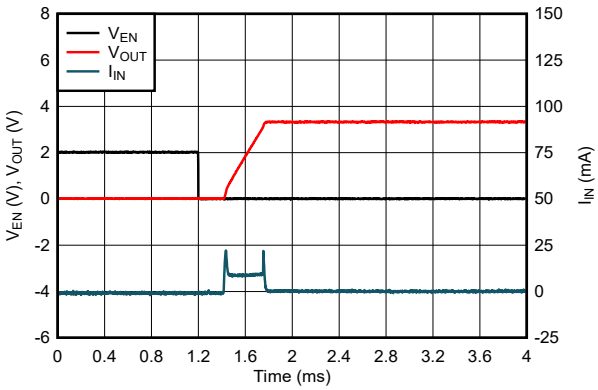



**Figure 7-7. LDO Start-Up Time With EN (New Chip)**

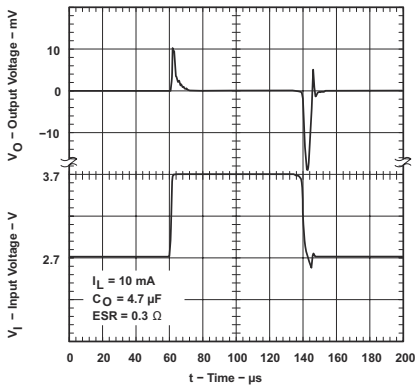



**Figure 7-8. TPS76915 Line Transient Response (Legacy Chip)**

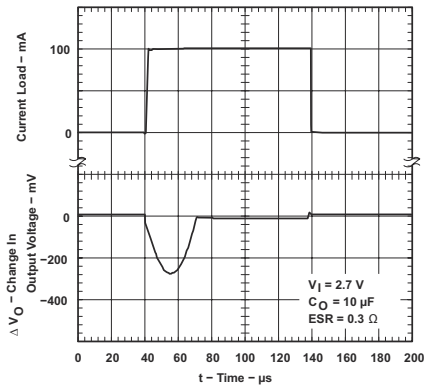



**Figure 7-9. TPS76915 Load Transient Response (Legacy Chip)**

### 7.2.3 Application Curves (continued)

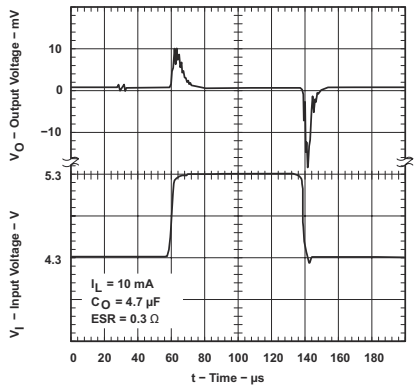
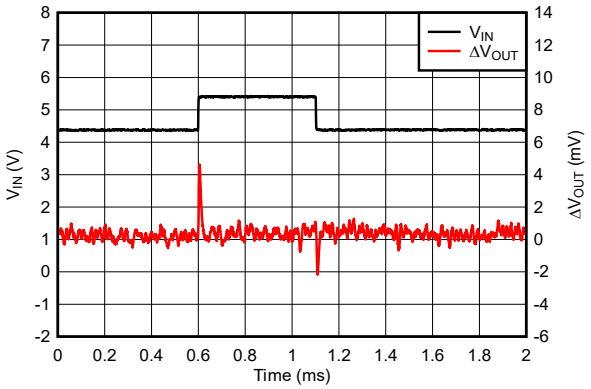
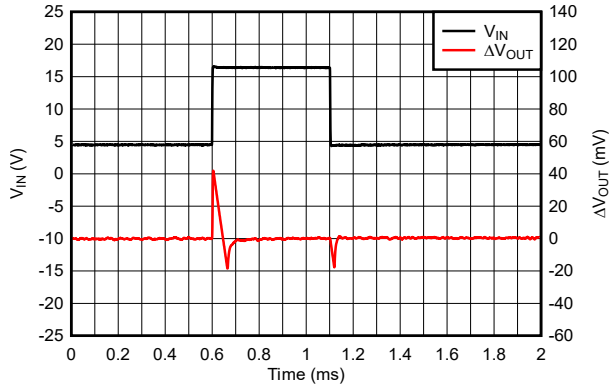



**Figure 7-10. TPS76933 Line Transient Response (Legacy Chip)**




4.3V to 5.3V at 1V/µs

**Figure 7-11. TPS76933 Line Transient Response (New Chip)**




4.3V to 16.0V at 1V/µs

**Figure 7-12. TPS76933 Line Transient Response (New Chip)**

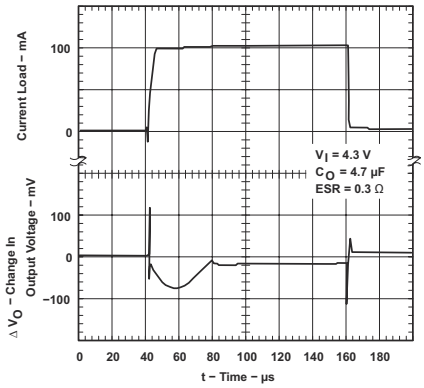
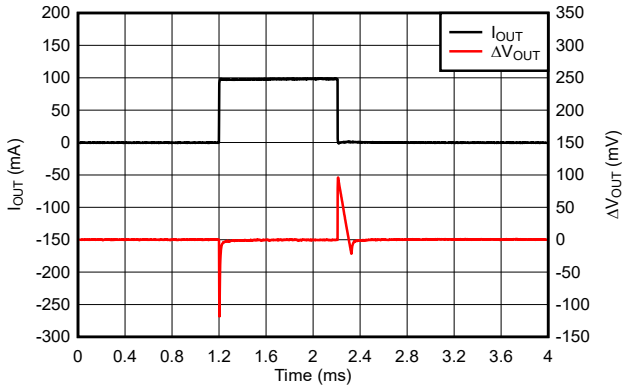
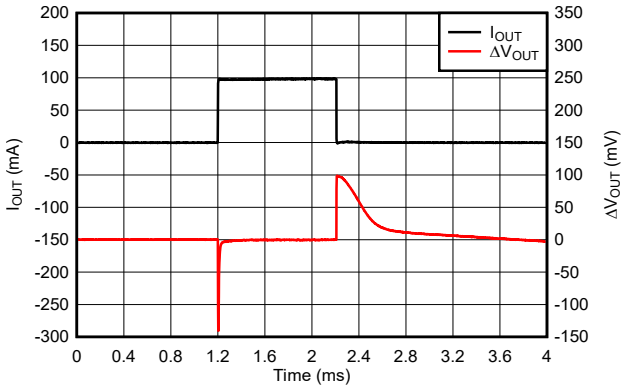



**Figure 7-13. TPS76933 Load Transient Response (Legacy Chip)**




1mA to 100mA at 1A/µs

**Figure 7-14. TPS76933 Load Transient Response (New Chip)**




1µA to 100mA at 1A/µs

**Figure 7-15. TPS76933 Load Transient Response (New Chip)**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### 7.2.3 Application Curves (continued)

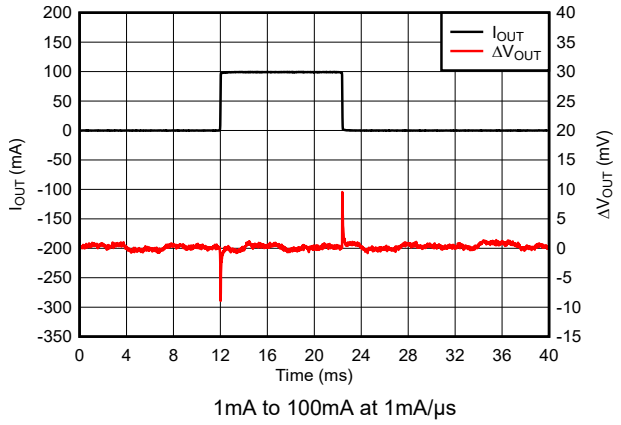


**Figure 7-16. TPS76933 Load Transient Response (New Chip)**

## 7.3 Power Supply Recommendations

The TPS769 is designed to operate from an input voltage supply range between 2.5V and 16V (new chip). The input voltage range provides adequate headroom for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR help improve the output noise performance.

## 7.4 Layout

### 7.4.1 Layout Guidelines

For the LDO power supply, especially high voltage and large current supplies, layout is an important step. If layout is not carefully designed, the regulator potentially does not deliver enough output current because of thermal limitation. Spread the GND layer as large as possible and place enough thermal vias on the thermal pad. These steps help improve device thermal performance, and maximize the current output at high ambient temperature. Figure 7-17 shows an example layout.

### 7.4.2 Layout Example

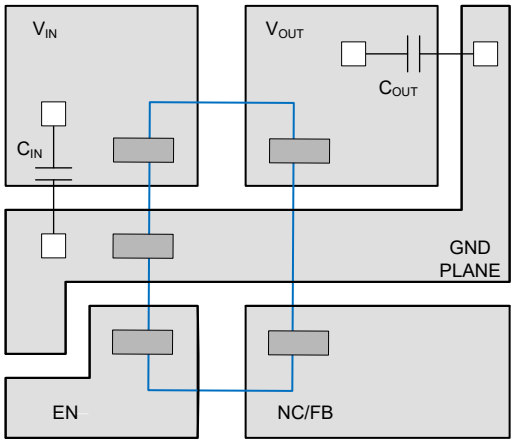


**Figure 7-17. Layout Recommendation**

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# 8 Device and Documentation Support

## 8.1 Device Support

### *8.1.1 Development Support*

#### 8.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS769. Request the TPS76901EVM-127 evaluation module (and related user's guide) at the TI website through the product folders or purchase directly from the TI eStore.

#### 8.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS769 is available through the product folders under *Tools & Software*.

#### 8.1.1.3 Device Nomenclature

**Table 8-1. Device Nomenclature**

| PRODUCT(1) | $V_{OUT}$ |
|---|---|
| TPS769**xxyyy**<br>Legacy chip | **xx** is the nominal output voltage (for example, 28 = 2.8V, 285 = 2.85V, and 01 = Adjustable).<br>**yyy** is the package designator.<br>**z** is the package quantity. |
| TPS769**xxyyyM3**<br>New chip | **xx** is the nominal output voltage (for example, 28 = 2.8V, 285 = 2.85V, and 01 = Adjustable).<br>**yyy** is the package designator.<br>**z** is the package quantity.<br>**M3** is a suffix designator for new chip redesigns on the latest TI process technology. |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

## 8.2 Documentation Support

### *8.2.1 Related Documentation*

For related documentation see the following:

- Texas Instruments, *TPS709-Q1 150-mA, 30-V, 1-µA IQ Voltage Regulators With Enable* data sheet
- Texas Instruments, *Universal LDO Evaluation Module* user guide
- Texas Instruments, *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note
- Texas Instruments, *Know Your Limits* application note

## 8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 8.5 Trademarks

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## 8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision E (May 2001) to Revision F (January 2025) | Page |
|---|---|
| • Updated the numbering format for tables, figures, and cross-references throughout the document | 1 |
| • Added the *Package Information*, *Pin Configuration and Functions*, *Specifications*, *ESD Ratings*, *Thermal Information*, *Detailed Description*, *Overview*, *Functional Block Diagram*, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Typical Applications*, *Power Supply Recommendations*, *Layout*, *Layout Guidelines*, *Layout Example*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections | 1 |
| • Removed *Available Options* table, see POA at the end of the data sheet | 1 |
| • Changed entire document to align with current family format | 1 |
| • Added M3 devices to document | 1 |

# 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS76901DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | PCFI |
| TPS76901DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | PCFI |
| TPS76901DBVRG4 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PCFI |
| TPS76901DBVRG4.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PCFI |
| TPS76912DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | PCGI |
| TPS76912DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PCGI |
| TPS76912DBVRG4 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PCGI |
| TPS76912DBVRG4.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PCGI |
| TPS76912DBVT | Obsolete | Production | SOT-23 (DBV) \| 5 | - | - | Call TI | Call TI | -40 to 125 | PCGI |
| TPS76915DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | PCHI |
| TPS76915DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | PCHI |
| TPS76915DBVRG4 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PCHI |
| TPS76918DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | PCII |
| TPS76918DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | PCII |
| TPS76918DBVRG4 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PCII |
| TPS76918DBVRG4.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PCII |
| TPS76925DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | PCJI |
| TPS76925DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | PCJI |
| TPS76925DBVT | Obsolete | Production | SOT-23 (DBV) \| 5 | - | - | Call TI | Call TI | -40 to 125 | PCJI |
| TPS76927DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PCKI |
| TPS76927DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PCKI |
| TPS76927DBVT | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PCKI |
| TPS76927DBVT.A | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PCKI |
| TPS76928DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PCLI |
| TPS76928DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PCLI |
| TPS76928DBVRG4 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PCLI |
| TPS76928DBVT | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PCLI |
| TPS76928DBVT.A | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PCLI |
| TPS76930DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | PCMI |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS76930DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | PCMI |
| TPS76930DBVRG4 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PCMI |
| TPS76930DBVRG4.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PCMI |
| TPS76930DBVT | Obsolete | Production | SOT-23 (DBV) \| 5 | - | - | Call TI | Call TI | -40 to 125 | PCMI |
| TPS76933DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | PCNI |
| TPS76933DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PCNI |
| TPS76933DBVRG4 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PCNI |
| TPS76933DBVRG4.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PCNI |
| TPS76933DBVT | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | PCNI |
| TPS76933DBVT.A | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PCNI |
| TPS76950DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | PCOI |
| TPS76950DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | PCOI |
| TPS76950DBVT | Obsolete | Production | SOT-23 (DBV) \| 5 | - | - | Call TI | Call TI | -40 to 125 | PCOI |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS769 :**

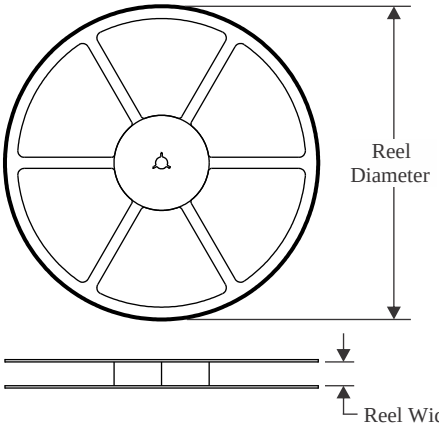
- Automotive : TPS769-Q1

NOTE: Qualified Version Definitions:

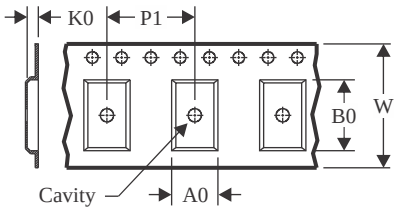
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

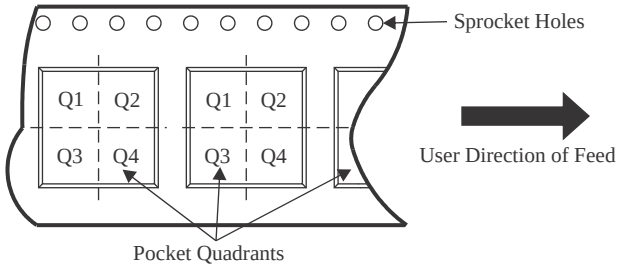



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

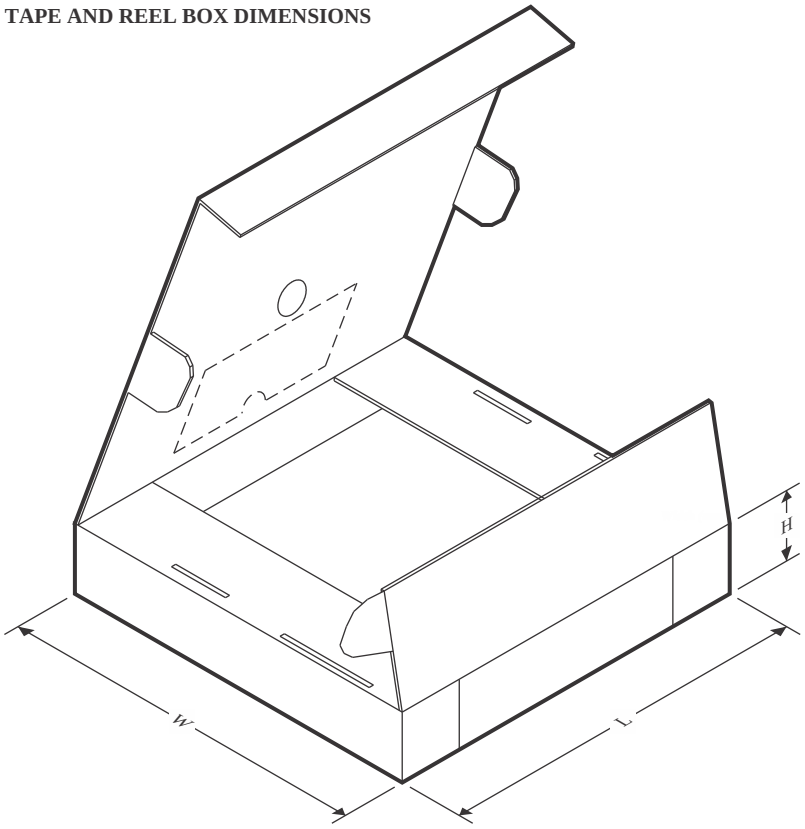



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS76901DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS76901DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS76901DBVRG4 | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS76912DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS76912DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS76912DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS76912DBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS76912DBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS76915DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS76915DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS76915DBVRG4 | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS76918DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS76918DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS76918DBVRG4 | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS76925DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS76925DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS76927DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS76927DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS76928DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS76928DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS76930DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS76930DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS76930DBVRG4 | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS76933DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS76933DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS76933DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS76933DBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS76933DBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS76933DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS76950DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS76950DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS76901DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS76901DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS76901DBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS76912DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS76912DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS76912DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS76912DBVRG4 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS76912DBVRG4 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS76915DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS76915DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS76915DBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS76918DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS76918DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS76918DBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS76925DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS76925DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS76927DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS76927DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |

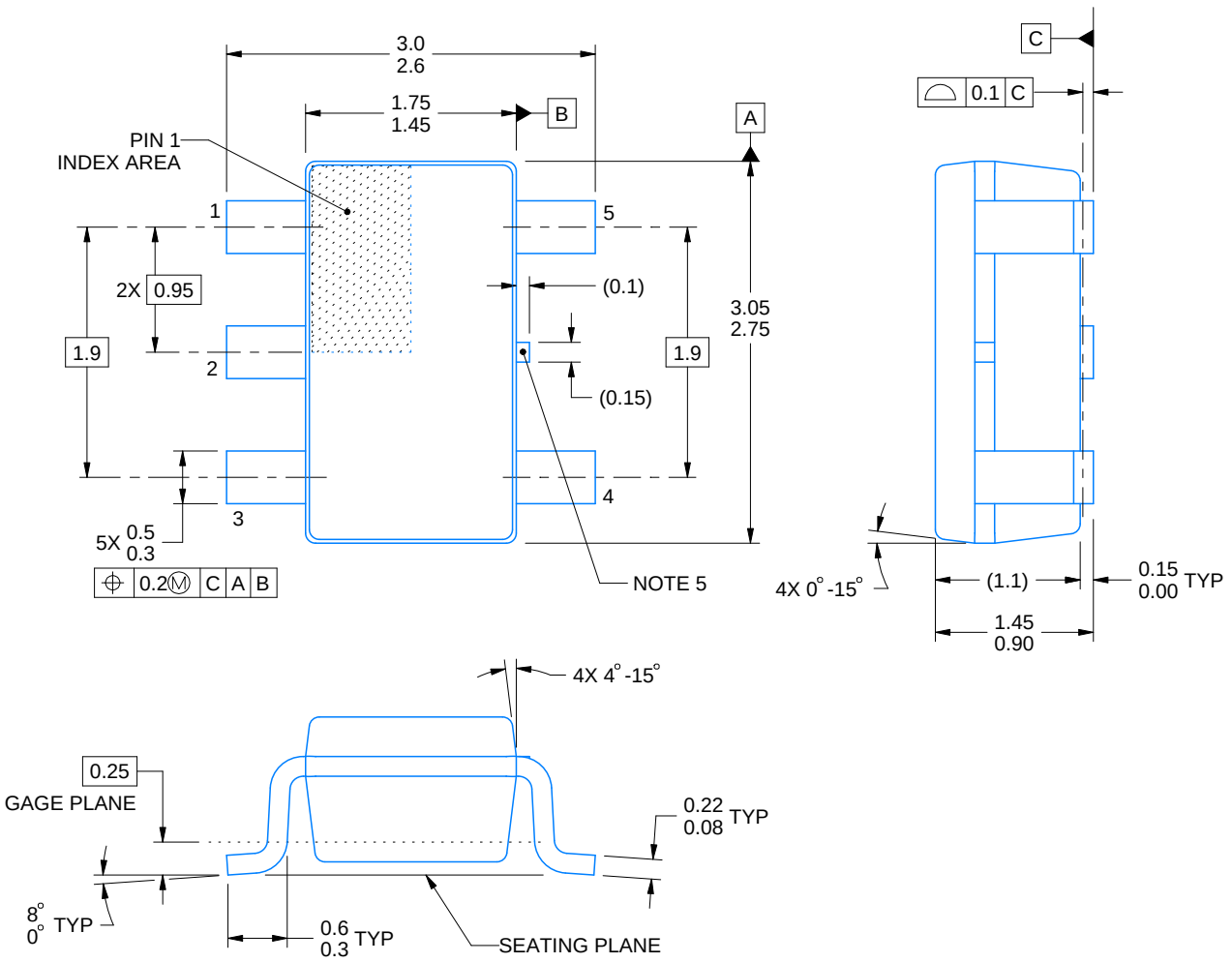
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS76928DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS76928DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS76930DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS76930DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS76930DBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS76933DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS76933DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS76933DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS76933DBVRG4 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS76933DBVRG4 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS76933DBVT | SOT-23 | DBV | 5 | 250 | 210.0 | 185.0 | 35.0 |
| TPS76950DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS76950DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

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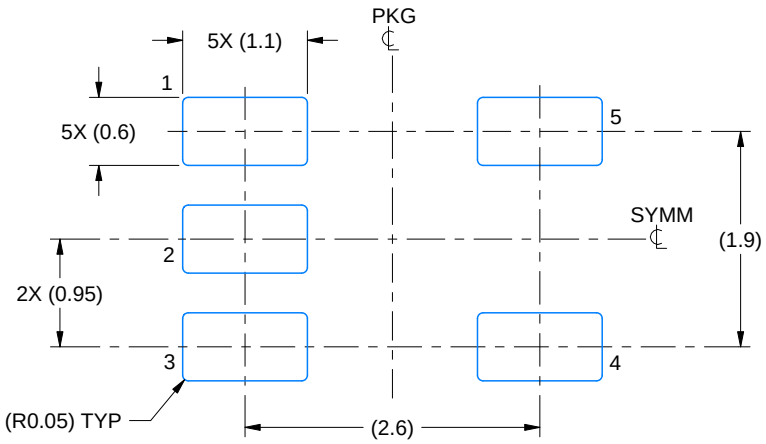
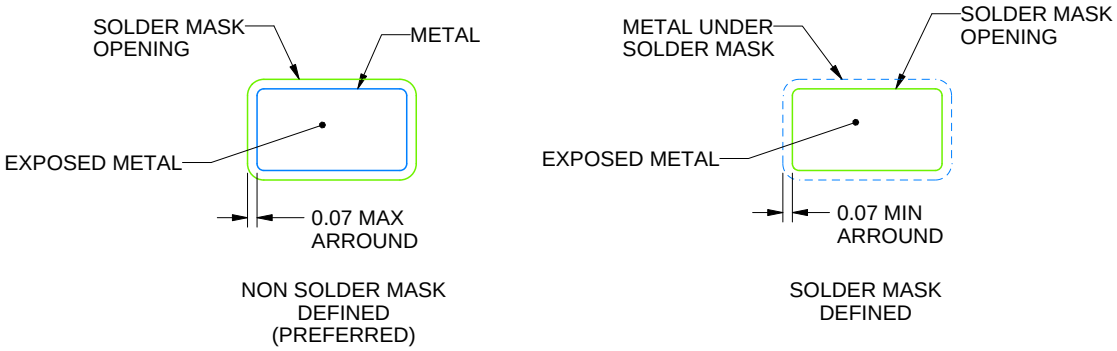
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X




SOLDER MASK DETAILS

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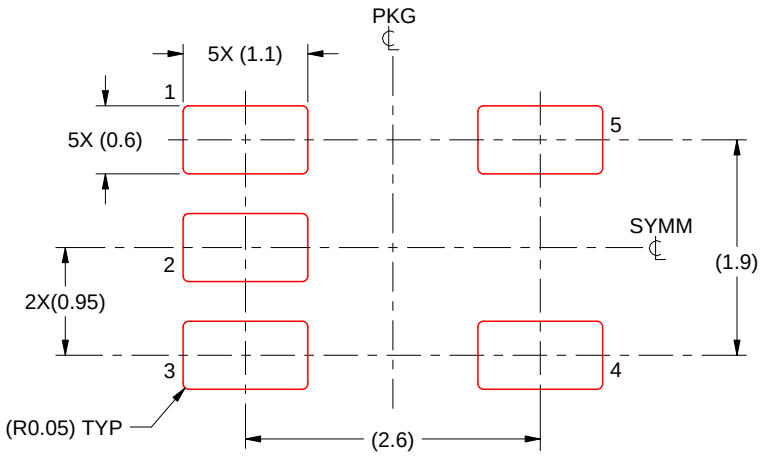
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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