ISO7821x High-Performance, 8000V_{PK} Reinforced Dual Channel Digital Isolator

1 Features

- Signaling Rate: Up to 100Mbps
- Wide Supply Range: 2.25V to 5.5V
- 2.25V to 5.5V Level Translation
- Wide Temperature Range: –55°C to 125°C
- Low Power Consumption, Typical 1.8mA per Channel at 1Mbps
- Low Propagation Delay: 11ns Typical (5V Supplies)
- Industry leading CMTI(Min): ±100kV/µs
- Robust Electromagnetic Compatibility (EMC)
- System-Level ESD, EFT, and Surge Immunity
- Low Emissions
- Isolation Barrier Life: > 25 Years
- SOIC-16 Wide Body (DW) and Extra-Wide Body (DWW) Package Options
- Safety and Regulatory Approvals:
  - 8000V_{PK} Reinforced Isolation per DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
  - 5.7kV_{RMS} Isolation for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 60601-1 End Equipment Standards
  - CQC Certification per GB4943.1-2011
  - TUV Certification per EN 61010-1 and EN 60950-1
  - All DW Package Certifications Complete; DWW Package Certifications Complete per UL, TUV and Planned for VDE, CSA, and CQC

2 Applications

- Industrial Automation
- Motor Control
- Power Supplies
- Solar Inverters
- Medical Equipment
- Hybrid Electric Vehicles

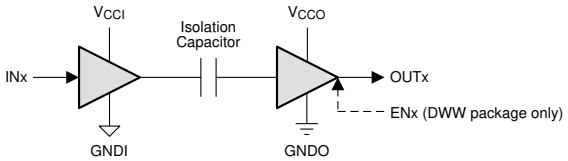
3 Description

The ISO7821 is a high-performance, dual-channel digital isolator with 8000V_{PK} isolation voltage. This device has reinforced isolation certifications according to VDE, CSA, CQC, and TUV. The isolator provides high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by silicon dioxide (SiO_2) insulation barrier. ISO7821 has one forward and one reverse-direction channel. If the input power or signal is lost, default output is 'high' for the ISO7821 and 'low' for the ISO7821F device. Used in conjunction with isolated power supplies, this device prevents noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. Through innovative chip design and layout techniques, electromagnetic compatibility of ISO7821 has been significantly enhanced to ease system-level ESD, EFT, Surge and Emissions compliance. ISO7821 is available in 16-pin SOIC wide-body (DW) and extra-wide body (DWW) packages. The DWW package option comes with enable pins which can be used to put the respective outputs in high impedance for multi-controller driving applications and to reduce power consumption.

Package Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)	PACKAGE SIZE(2)
ISO7821, ISO7821F	DW (SOIC, 16)	10.30mm × 7.50mm	10.30mm × 10.30mm
	DWW (Extra wide SOIC, 16)	10.30mm × 14.0mm	10.30mm × 17.25mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



A. V_{CCI} and GNDI are supply and ground connections respectively for the input channels.
B. V_{CCO} and GNDO are supply and ground connections respectively for the output channels.

Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

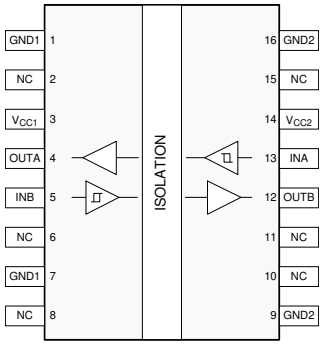


Figure 4-1. DW Package 16-Pin (SOIC) Top View

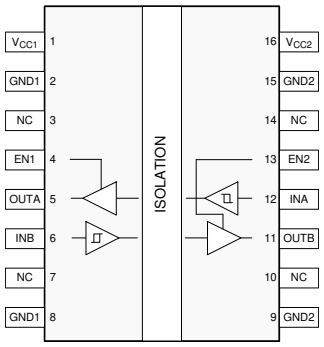


Figure 4-2. DWW Package 16-Pin (SOIC) Top View

Table 4-1. Pin Functions

PIN			Type	DESCRIPTION
NAME	NO.	NO.		
	DW	DWW		
GND1	1, 7	2,8	–	Ground connection for V_{CC1}
GND2	9, 16	9,15	–	Ground connection for V_{CC2}
INA	13	12	I	Input, channel A
INB	5	6	I	Input, channel B
NC	2, 6, 8, 10 ,11, 15	3,7,10,14	–	Not connected
OUTA	4	5	O	Output, channel A
OUTB	12	11	O	Output, channel B
V_{CC1}	3	1	–	Power supply, V_{CC1}
V_{CC2}	14	16	–	Power supply, V_{CC2}
EN1	–	4	I	Output enable 1. Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low.
EN2	–	13	I	Output enable 2. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low.

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5 Specifications

5.1 Absolute Maximum Ratings

(1)		MIN	MAX	UNIT
Supply voltage(2)	V_{CC1}, V_{CC2}	–0.5	6	V
Voltage	INx, OUTx	–0.5	V_{CC} + 0.5(3)	V
Output Current	I_O	-15	15	mA
Surge Immunity			12.8	kV
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

5.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±6000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage		2.25		5.5	V
I_{OH}	High-level output current	V_{CCO} (2) = 5 V	-4			mA
		V_{CCO} = 3.3 V	-2			
		V_{CCO} = 2.5 V	-1			
I_{OL}	Low-level output current	V_{CCO} = 5 V			4	mA
		V_{CCO} = 3.3 V			2	
		V_{CCO} = 2.5 V			1	
V_{IH}	High-level input voltage		0.7 x $V_{CC\ I}$ (2)		V_{CCI}	V
V_{IL}	Low-level input voltage		0		0.3 x V_{CCI}	V
DR	Signaling rate		0		100	Mbps
T_J	Junction temperature(1)		-55		150	°C
T_A	Ambient temperature		-55	25	125	°C

(1) To maintain the recommended operating conditions for T_J, see the *Thermal Information* table.
(2) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

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5.4 Thermal Information

THERMAL METRIC[1]		ISO7821		UNIT
		DW (SOIC)	DWW (SOIC)	
		16 PINS	16-PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.7	84.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	47.3	46.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.4	54.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	19.1	18.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	48.8	53.8	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Power Dissipation Characteristics

			VALUE	UNIT
P_D	Maximum power dissipation by ISO7821	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, input a 50 MHz 50% duty cycle square wave	100	mW
P_{D1}	Maximum power dissipation by side-1 of ISO7821 x		50	
P_{D2}	Maximum power dissipation by side-2 of ISO7821 x		50	

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5.6 Electrical Characteristics, 5 V

V_{CC1} = V_{CC2} = 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 6-1	V_{CCO} (1) – 0.4	V_{CCO} – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 6-1		0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCO} (1)			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	-10			
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V; see Figure 6-4	100			kV/µs
Supply Current - ISO7821DW and ISO7821FDW						
I_{CC1}, I_{CC2}	DC Signal	V_I = 0 V (ISO7821F) , V_I = V_{CCI} (1) (ISO7821)		1.2	1.7	mA
I_{CC1}, I_{CC2}	DC Signal	V_I = V_{CCI} (1) (ISO7821F) , V_I = 0 V (ISO7821)		2.4	3.4	mA
I_{CC1}, I_{CC2}	1 Mbps	All channels switching with square wave clock input; C_L = 15 pF		1.8	2.6	mA
I_{CC1}, I_{CC2}	10 Mbps			2.4	3.2	mA
I_{CC1}, I_{CC2}	100 Mbps			7.5	9.3	mA
Supply Current - ISO7821DWW and ISO7821FDWW						
I_{CC1}, I_{CC2}	Disable	EN1 = EN2 = 0V, V_I = 0 V (ISO7821F) , V_I = V_{CCI} (1)(ISO7821)		0.7	1.1	mA
I_{CC1}, I_{CC2}	Disable	EN1 = EN2 = 0V, V_I = V_{CCI} (1) (ISO7821F) , V_I = 0 V (ISO7821)		1.8	2.9	mA
I_{CC1}, I_{CC2}	DC Signal	V_I = 0 V (ISO7821F) , V_I = V_{CCI} (1) (ISO7821)		1.2	1.7	mA
I_{CC1}, I_{CC2}	DC Signal	V_I = V_{CCI} (1) (ISO7821F) , V_I = 0 V (ISO7821)		2.4	3.5	mA
I_{CC1}, I_{CC2}	1 Mbps	All channels switching with square wave clock input; C_L = 15 pF		1.9	2.7	mA
I_{CC1}, I_{CC2}	10 Mbps			2.5	3.2	mA
I_{CC1}, I_{CC2}	100 Mbps			7.7	9.3	mA

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

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5.7 Electrical Characteristics, 3.3 V

V_{CC1} = V_{CC2} = 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA; see Figure 6-1	V_{CCO} (1) – 0.4	V_{CCO} – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA; see Figure 6-1		0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCO}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	-10			
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V; see Figure 6-4	100			kV/µs
Supply Current - ISO7821DW and ISO7821FDW						
I_{CC1}, I_{CC2}	DC Signal	V_I = 0 V (ISO7821F) , V_I = V_{CCI} (1) (ISO7821)		1.2	1.7	mA
I_{CC1}, I_{CC2}	DC Signal	V_I = V_{CCI} (1) (ISO7821F) , V_I = 0 V (ISO7821)		2.4	3.4	mA
I_{CC1}, I_{CC2}	1 Mbps	All channels switching with square wave clock input; C_L = 15 pF		1.8	2.6	mA
I_{CC1}, I_{CC2}	10 Mbps			2.2	3	mA
I_{CC1}, I_{CC2}	100 Mbps			5.8	7.1	mA
Supply Current - ISO7821DWW and ISO7821FDWW						
I_{CC1}, I_{CC2}	Disable	EN1 = EN2 = 0V, V_I = 0 V (ISO7821F) , V_I = V_{CCI} (1)(ISO7821)		0.7	1.1	mA
I_{CC1}, I_{CC2}	Disable	EN1 = EN2 = 0V, V_I = V_{CCI} (1) (ISO7821F) , V_I = 0 V (ISO7821)		1.8	2.9	mA
I_{CC1}, I_{CC2}	DC Signal	V_I = 0 V (ISO7821F) , V_I = V_{CCI} (1) (ISO7821)		1.2	1.7	mA
I_{CC1}, I_{CC2}	DC Signal	V_I = V_{CCI} (1) (ISO7821F) , V_I = 0 V (ISO7821)		2.4	3.5	mA
I_{CC1}, I_{CC2}	1 Mbps	All channels switching with square wave clock input; C_L = 15 pF		1.9	2.6	mA
I_{CC1}, I_{CC2}	10 Mbps			2.3	3	mA
I_{CC1}, I_{CC2}	100 Mbps			5.9	7.1	mA

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

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5.8 Electrical Characteristics, 2.5 V

V_{CC1} = V_{CC2} = 2.5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA; see Figure 6-1	V_{CCO} (1) – 0.4	V_{CCO} – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA; see Figure 6-1		0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCO}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	-10			
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V; see Figure 6-4	100			kV/µs
Supply Current - ISO7821DW and ISO7821FDW						
I_{CC1}, I_{CC2}	DC Signal	V_I = 0 V (ISO7821F) , V_I = V_{CCI} (1) (ISO7821)		1.2	1.7	mA
I_{CC1}, I_{CC2}	DC Signal	V_I = V_{CCI} (1) (ISO7821F) , V_I = 0 V (ISO7821)		2.4	3.4	mA
I_{CC1}, I_{CC2}	1 Mbps	All channels switching with square wave clock input; C_L = 15 pF		1.8	2.6	mA
I_{CC1}, I_{CC2}	10 Mbps			2.1	2.8	mA
I_{CC1}, I_{CC2}	100 Mbps			4.9	5.9	mA
Supply Current - ISO7821DWW and ISO7821FDWW						
I_{CC1}, I_{CC2}	Disable	EN1 = EN2 = 0V, V_I = 0 V (ISO7821F) , V_I = V_{CCI} (1)(ISO7821)		0.7	1.1	mA
I_{CC1}, I_{CC2}	Disable	EN1 = EN2 = 0V, V_I = V_{CCI} (1) (ISO7821F) , V_I = 0 V (ISO7821)		1.8	2.9	mA
I_{CC1}, I_{CC2}	DC Signal	V_I = 0 V (ISO7821F) , V_I = V_{CCI} (1) (ISO7821)		1.2	1.7	mA
I_{CC1}, I_{CC2}	DC Signal	V_I = V_{CCI} (1) (ISO7821F) , V_I = 0 V (ISO7821)		2.4	3.5	mA
I_{CC1}, I_{CC2}	1 Mbps	All channels switching with square wave clock input; C_L = 15 pF		1.9	2.6	mA
I_{CC1}, I_{CC2}	10 Mbps			2.2	2.9	mA
I_{CC1}, I_{CC2}	100 Mbps			5	6	mA

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

5.9 Power Ratings

Table 5-1. IEC 60664-1 Ratings Table

PARAMETER		TEST CONDITIONS	SPECIFICATION
Material group			I
Overvoltage category / Installation classification	DW package	Rated mains voltage ≤ 600 V_{RMS}	I–IV
		Rated mains voltage ≤ 1000 V_{RMS}	I–III
	DWW package	Rated mains voltage ≤ 1000 V_{RMS}	I–IV

5.10 Insulation Specifications

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Table 5-2. Insulation Characteristics

PARAMETER		TEST CONDITIONS	SPECIFICATION		UNIT
			DW	DWW	
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	21	21	µm
V_{IOWM}	Maximum working isolation voltage	Time dependent dielectric breakdown (TDDB) test	1500	2000	V_{RMS}
			2121	2828	V_{DC}
DIN V VDE V 0884-10 (VDE V 0884-10):2006-12					
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$ t = 60 sec (qualification) t= 1 sec (100% production)	8000	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage	Test method per IEC 60065, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 12800\ V_{PK}$ (1) (qualification)	8000	8000	V_{PK}
V_{IORM}	Maximum repetitive peak isolation voltage		2121	2828	V_{PK}
V_{PR}	Input-to-output test voltage	Method a, After Input/Output safety test subgroup 2/3, $V_{PR} = V_{IORM} \times 1.2$, t = 10 s, Partial discharge < 5 pC	2545	3394	V_{PK}
		Method a, After environmental tests subgroup 1, $V_{PR} = V_{IORM} \times 1.6$, t = 10 s, Partial Discharge < 5 pC	3394	4525	
		Method b1,After environmental tests subgroup 1, $V_{PR} = V_{IORM} \times 1.875$, t = 1 s (100% Production test) Partial discharge < 5 pC	3977	5303	
R_S	Isolation resistance	V_{IO} = 500 V at T_S	$>10^9$	$>10^9$	Ω
	Pollution degree		2	2	
	Climatic category		55/125/21	55/125/21	
UL 1577					
V_{ISO}	Withstanding isolation voltage	$V_{TEST} = V_{ISO} = 5700\ V_{RMS}$, t = 60 sec (qualification); $V_{TEST} = 1.2 \times V_{ISO} = 6840\ V_{RMS}$, t = 1 sec (100% production)	5700	5700	V_{RMS}

(1) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.

Table 5-3. Package Insulation and Safety-Related Specifications

(over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
CLR	External clearance	Shortest terminal-to-terminal distance through air	DW-16	8.15			mm
			DWW-16	14.5	15.0		
CPG	External creepage	Shortest terminal-to-terminal distance across the package surface	DW-16	8.15			mm
			DWW-16	14.5	15.0		
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112; UL 746A		600			V
R_{IO}	Isolation resistance, input to output(1)	V_{IO} = 500 V, T_A = 25°C		10^{12}			Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ max		10^{11}			Ω
C_{IO}	Barrier capacitance, input to output(1)	V_{IO} = 0.4 x sin (2πft), f = 1 MHz			1		pF
C_I	Input capacitance(2)	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft)$, f = 1 MHz, V_{CC} = 5 V			2		pF

(1) All pins on each side of the barrier tied together creating a two-terminal device.
(2) Measured from input pin to ground.

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Note

Creepage and clearance requirements must be applied according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to verify that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

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5.11 Safety-Related Certifications

DW package certifications are complete; DWW package certifications completed for UL and TUV and planned for VDE, CSA, and CQC.

Table 5-4. Regulatory Information

VDE	CSA	UL	CQC	TUV
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 60950-1 (VDE 0805 Teil 1):2011-01	Approved under CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 60601-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB 4943.1-2011	Certified according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A11:2009/ A1:2010/A12:2011/A2:2013
Reinforced insulation Maximum transient isolation voltage, 8000 V_{PK}; Maximum repetitive peak isolation voltage, 2121 V_{PK} (DW), 2828 V_{PK} (DWW); Maximum surge isolation voltage, 8000 V_{PK}	Reinforced insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed., 800 V_{RMS} (DW package) and 1450 V_{RMS} (DWW package) max working voltage (pollution degree 2, material group I); 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3.1, 250 V_{RMS} (354 V_{PK}) max working voltage (DW package)	Single protection, 5700 V_{RMS}	Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V_{RMS} maximum working voltage	5700 V_{RMS} Reinforced insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of 600 V_{RMS} (DW package) and 1000 V_{RMS} (DWW package) 5700 V_{RMS} Reinforced insulation per EN 60950-1:2006/A11:2009/ A1:2010/A12:2011/A2:2013 up to working voltage of 800 V_{RMS} (DW package) and 1450 V_{RMS} (DWW package)
Certificate number: 40040142	Master contract number: 220991	File number: E181974	Certificate number: CQC15001121716	Client ID number: 77311

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5.12 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

Table 5-5. Safety Limiting

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current for DW-16 package and DWW-16 Packages	$R_{\theta JA}$ = 84.7°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			268	mA
		$R_{\theta JA}$ = 84.7°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			410	
		$R_{\theta JA}$ = 84.7°C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C			537	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 84.7°C/W, T_J = 150°C, T_A = 25°C			1476	mW
T_S	Maximum safety temperature				150	°C

The maximum safety temperature is the maximum junction temperature specified for the device. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Section 5.4* is that of a device installed on a High-K test board for Leaded Surface Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

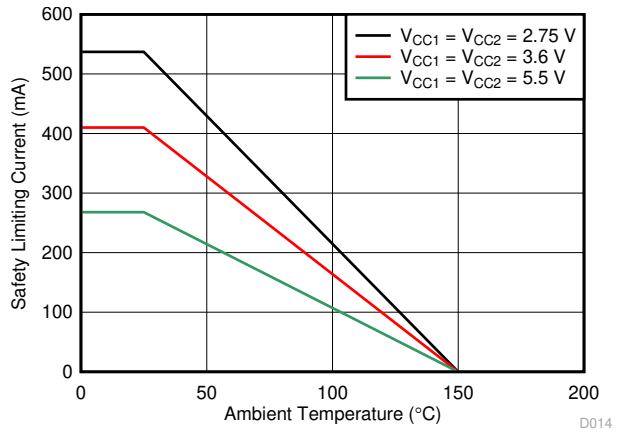


Figure 5-1. Thermal Derating Curve for Safety Limiting Current per VDE

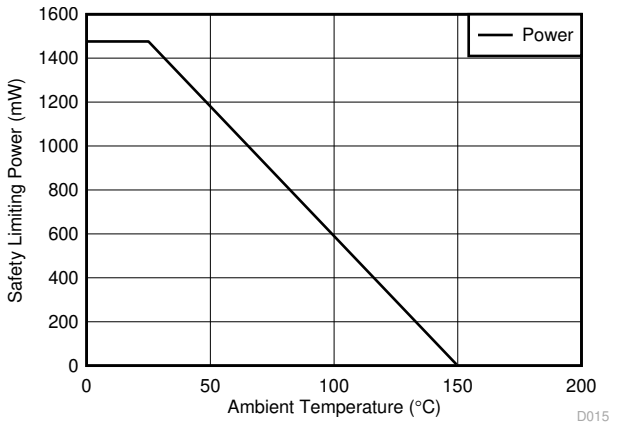


Figure 5-2. Thermal Derating Curve for Safety Limiting Power per VDE

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5.13 Switching Characteristics, 5 V

V_{CC1} = V_{CC2} = 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 6-1	6	10.7	16	ns
PWD(1)	Pulse width distortion $\|t_{PHL} - t_{PLH}\|$			0.6	4.6	
$t_{sk(pp)}$ (2)	Part-to-part skew time				4.5	ns
t_r	Output signal rise time	See Figure 6-1		2.4	3.9	ns
t_f	Output signal fall time			2.4	3.9	
t_{PHZ}	Disable propagation delay, high-to-high impedance output for ISO7821DWW and ISO7821FDWW	See Figure 6-2		12	20	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output for ISO7821DWW and ISO7821FDWW			12	20	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO7821DWW			10	20	ns
	Enable propagation delay, high impedance-to-high output for ISO7821FDWW			2	2.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO7821DWW			2	2.5	µs
	Enable propagation delay, high impedance-to-low output for ISO7821FDWW			10	20	ns
t_{fs}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 6-3		0.2	9	µs
t_{ie}	Time interval error	2^{16} - 1 PRBS data at 100 Mbps		1		ns

(1) Also known as Pulse Skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

5.14 Switching Characteristics, 3.3 V

V_{CC1} = V_{CC2} = 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 6-1	6	10.8	16	ns
PWD(1)	Pulse width distortion $\|t_{PHL} - t_{PLH}\|$			0.7	4.7	
$t_{sk(pp)}$ (2)	Part-to-part skew time				4.5	ns
t_r	Output signal rise time	See Figure 6-1		1.3	3	
t_f	Output signal fall time			1.3	3	
t_{PHZ}	Disable propagation delay, high-to-high impedance output for ISO7821DWW and ISO7821FDWW	See Figure 6-2		17	32	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output for ISO7821DWW and ISO7821FDWW			17	32	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO7821DWW			17	32	ns
	Enable propagation delay, high impedance-to-high output for ISO7821FDWW			2	2.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO7821DWW			2	2.5	µs
	Enable propagation delay, high impedance-to-low output for ISO7821FDWW			17	32	ns
t_{fs}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 6-3		0.2	9	µs
t_{ie}	Time interval error	2^{16} - 1 PRBS data at 100 Mbps		1		ns

(1) Also known as Pulse Skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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5.15 Switching Characteristics, 2.5 V

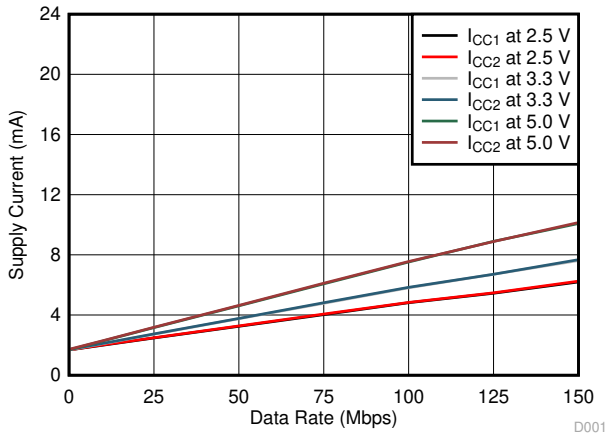
V_{CC1} = V_{CC2} = 2.5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 6-1	7.5	11.7	17.5	ns
PWD(1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$			0.7	4.7	
$t_{sk(pp)}$ (2)	Part-to-part skew time				4.5	ns
t_r	Output signal rise time	See Figure 6-1		1.8	3.5	
t_f	Output signal fall time			1.8	3.5	
t_{PHZ}	Disable propagation delay, high-to-high impedance output for ISO7821DWW and ISO7821FDWW	See Figure 6-2		22	45	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output for ISO7821DWW and ISO7821FDWW			22	45	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO7821DWW			18	45	ns
	Enable propagation delay, high impedance-to-high output for ISO7821FDWW			2	2.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO7821DWW			2	2.5	µs
	Enable propagation delay, high impedance-to-low output for ISO7821FDWW			18	45	ns
t_{fs}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 6-3		0.2	9	µs
t_{ie}	Time interval error	2^{16} - 1 PRBS data at 100 Mbps		1		ns

(1) Also known as Pulse Skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

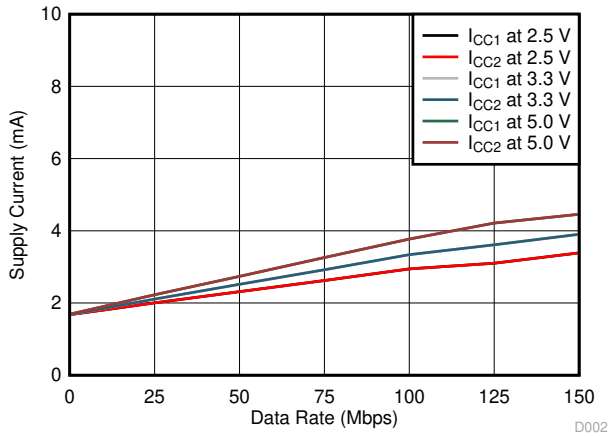
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5.16 Typical Characteristics



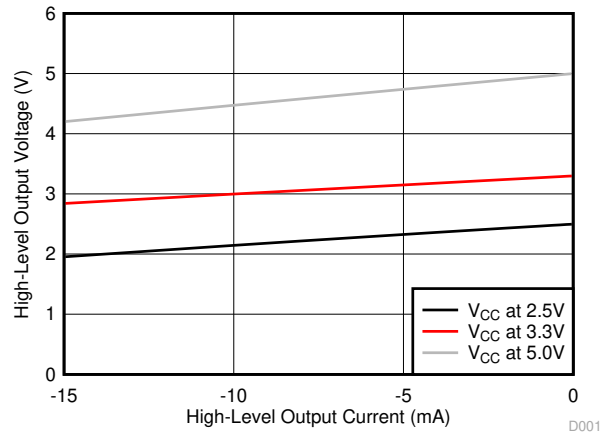
T_A = 25°C C_L = 15 pF

Figure 5-3. Supply Current vs Data Rate (With 15 pF Load)



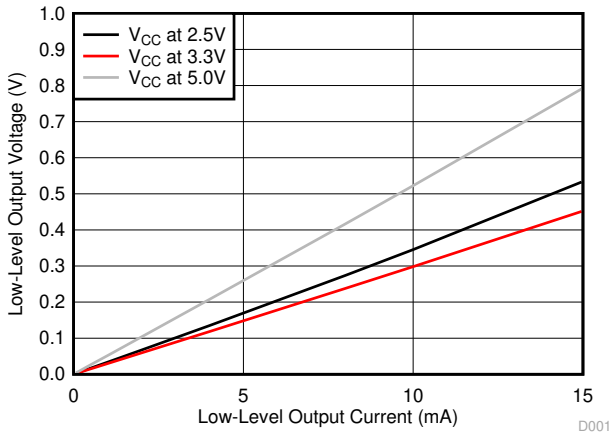
T_A = 25°C C_L = No Load

Figure 5-4. Supply Current vs Data Rate (With No Load)



T_A = 25°C

Figure 5-5. High-Level Output Voltage vs High-level Output Current



T_A = 25°C

Figure 5-6. Low-Level Output Voltage vs Low-Level Output Current

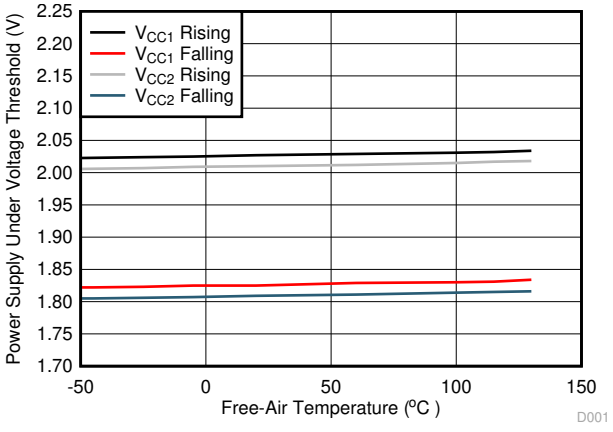


Figure 5-7. Power Supply Undervoltage Threshold vs Free-Air Temperature

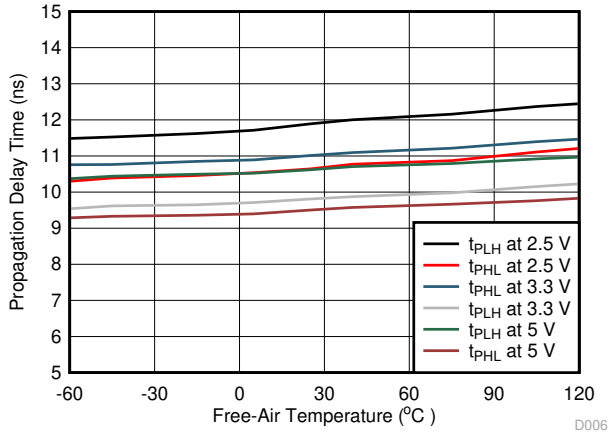
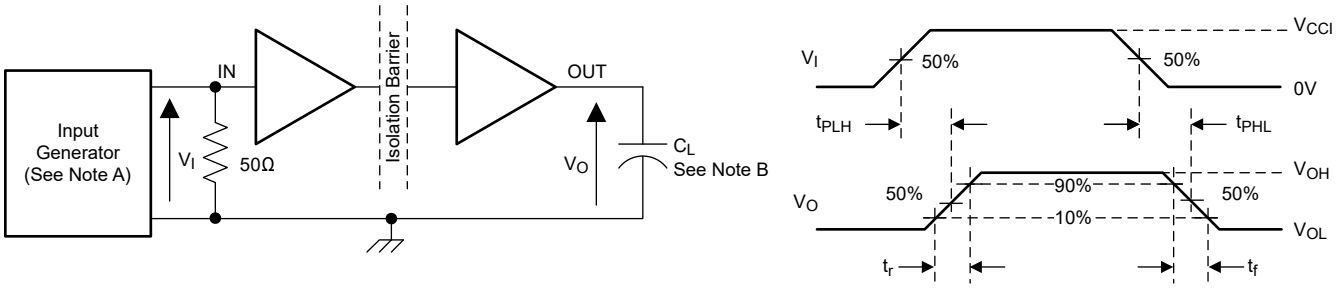


Figure 5-8. Propagation Delay Time vs Free-Air Temperature

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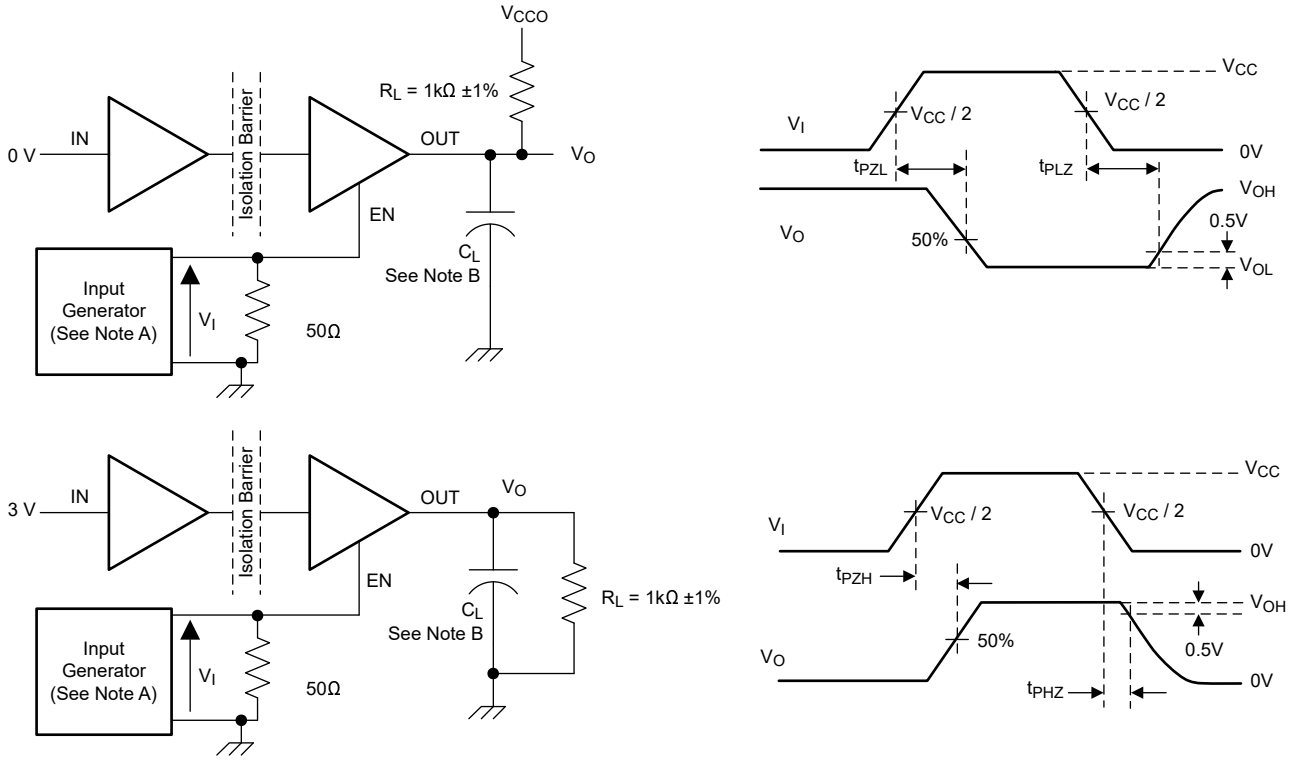
6 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. The 50 Ω resistor is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 6-1. Switching Characteristics Test Circuit and Voltage Waveforms

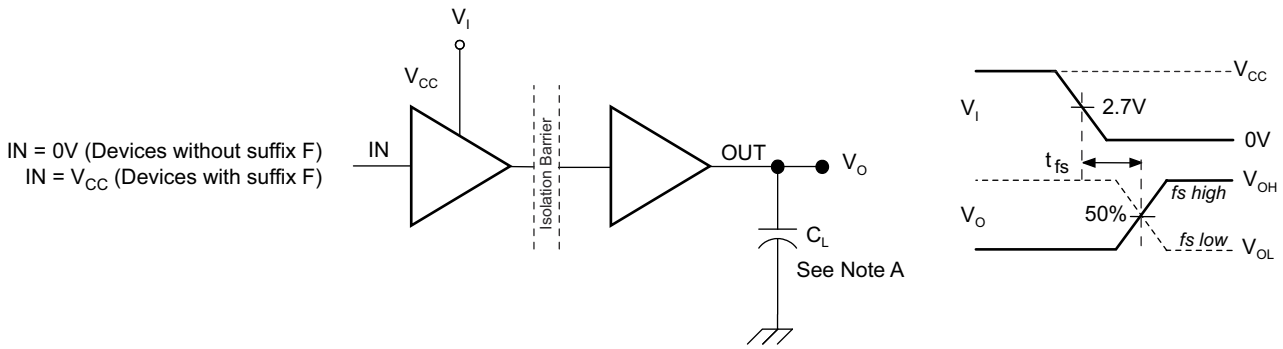


A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

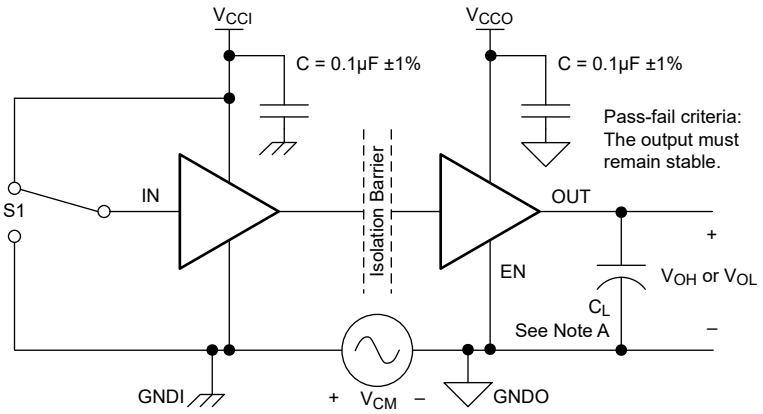
Figure 6-2. Enable/Disable Propagation Delay Time Test Circuit and Waveform

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A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 6-3. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 6-4. Common-Mode Transient Immunity Test Circuit

7 Detailed Description

7.1 Overview

ISO7821 employs an ON-OFF Keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. These devices also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Figure 7-1, shows a functional block diagram of a typical channel.

7.2 Functional Block Diagram

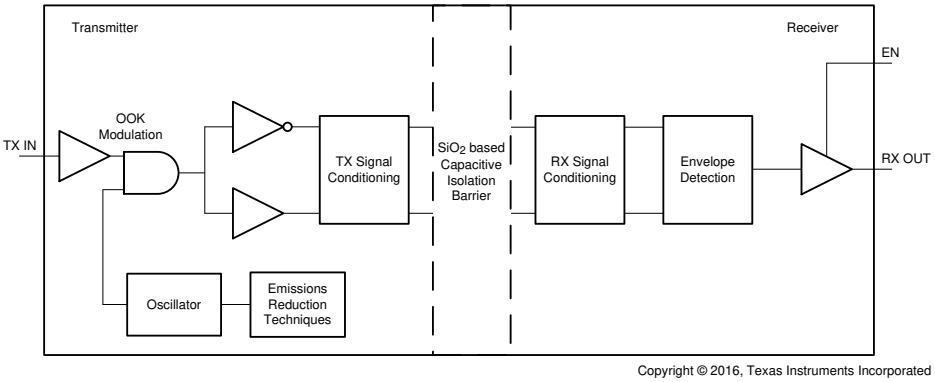


Figure 7-1. Conceptual Block Diagram of a Digital Capacitive Isolator

Also a conceptual detail of how the ON/OFF Keying scheme works is shown in Figure 7-2.

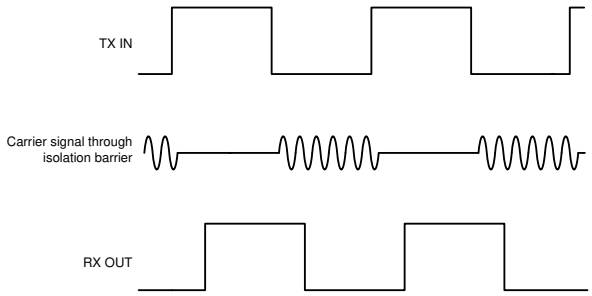


Figure 7-2. On-Off Keying (OOK) Based Modulation Scheme

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7.3 Feature Description

ISO7821 is available in two channel configurations and default output state options to enable a variety of application uses.

PRODUCT	CHANNEL DIRECTION	RATED ISOLATION	MAX DATA RATE	DEFAULT OUTPUT
ISO7821	1 Forward, 1 Reverse	5700 V_{RMS} / 8000 V_{PK} (1)	100 Mbps	High
ISO7821F	1 Forward, 1 Reverse	5700 V_{RMS} / 8000 V_{PK} (1)	100 Mbps	Low

(1) See the *Regulatory Information* section for detailed isolation ratings.

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7.4 Device Functional Modes

ISO7821 functional modes are shown in Table 7-1.

Table 7-1. ISO7821 Function Table

V_{CCI}	V_{CCO}	INPUT (INx)(2)	OUTPUT ENABLE (ENx) (DWW Package Only)	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H or open	H	Normal Operation: A channel output assumes the logic state of the input.
		L	H or open	L	
		Open	H or open	Default	Default mode: When INx is open, the corresponding channel output goes to the default high logic state. Default= High for ISO7821 and Low for ISO7821F.
X	PU	X	L	Z	A low value of Output Enable causes the outputs to be high-impedance.
PD	PU	X	H or open	Default	Default mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default= High for ISO7821 and Low for ISO7821F. When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	X	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined (1). When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input

(1) The outputs are in undetermined state when 1.7 V < V_{CCI}, V_{CCO} < 2.25 V.
(2) A strongly driven input signal can weakly power the floating V_{CC} using an internal protection diode and cause undetermined output.

7.4.1 Device I/O Schematics

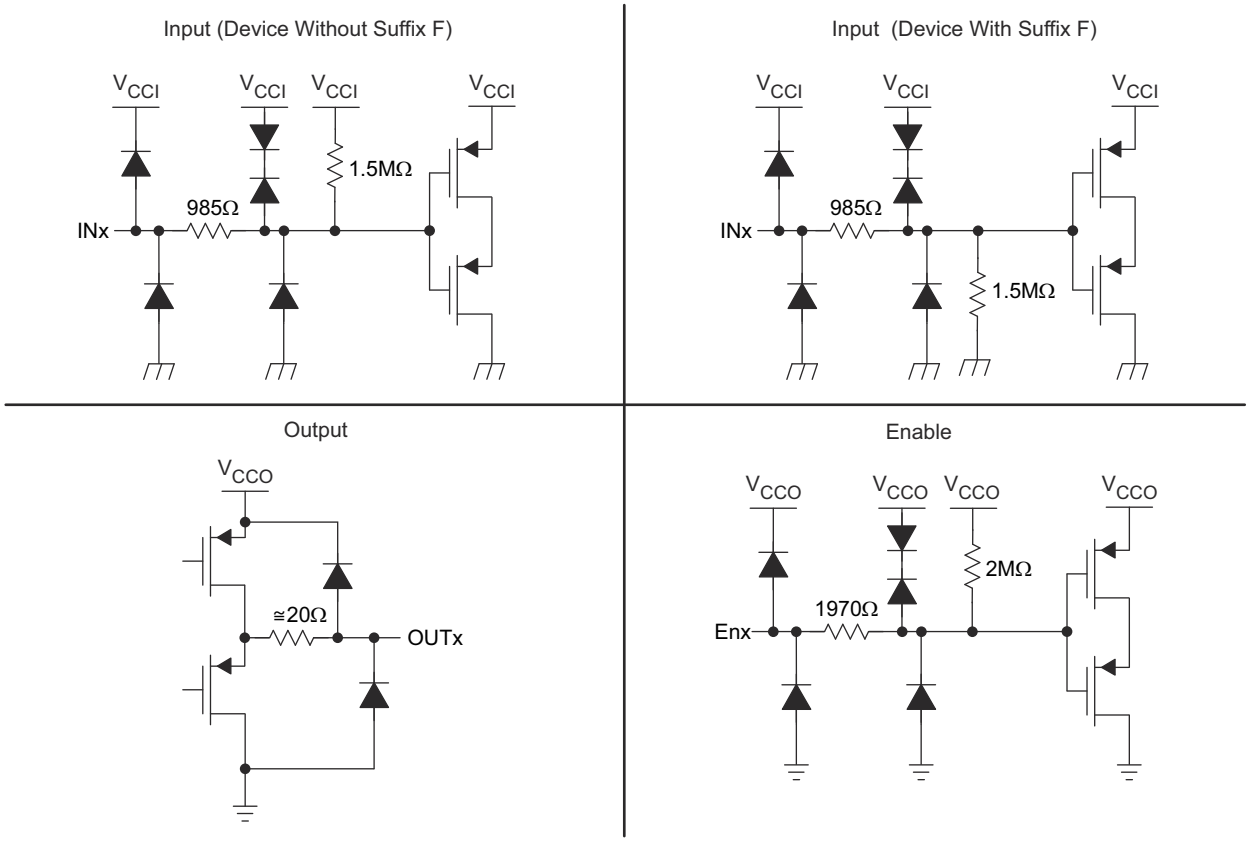


Figure 7-3. Device I/O Schematics

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The ISO7821 is a high-performance, dual-channel digital isolator with 5.7 kV_{RMS} isolation voltage per UL 1577. The device uses single-ended CMOS-logic switching technology. The supply voltage range is from 2.25 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. Keep in mind that when designing with digital isolators, due to the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

8.2 Typical Application

ISO782 1 can be used with Texas Instruments' mixed signal micro-controller, digital-to-analog converter, transformer driver, and voltage regulator to create an isolated 4-20 mA current loop .

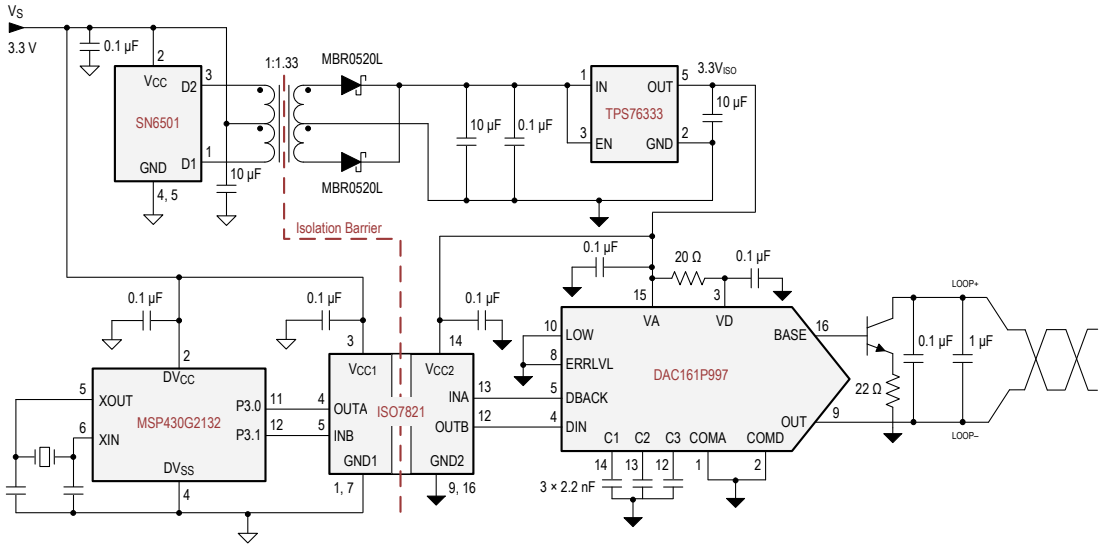


Figure 8-1. Isolated 4-20 mA Current Loop

8.2.1 Design Requirements

For the ISO7821, use the parameters shown in Table 8-1.

Table 8-1. Design Parameters

PARAMETER	VALUE
Supply voltage	2.25 V to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 µF
Decoupling capacitor from V_{CC2} and GND2	0.1 µF

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8.2.2 Detailed Design Procedure

Unlike optocouplers, which need external components to improve performance, provide bias, or limit current, ISO7821 only needs two external bypass capacitors to operate.

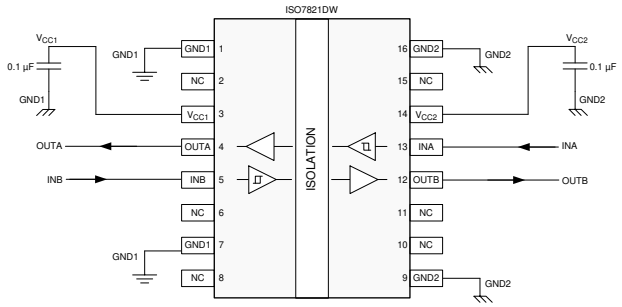


Figure 8-2. Typical ISO7821 Circuit Hook-up

8.2.2.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO7821 incorporate many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by providing purely differential internal operation.

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8.2.3 Application Performance Curve

Typical eye diagram of ISO7821 indicate low jitter and wide open eye at the maximum data rate of 100 Mbps.

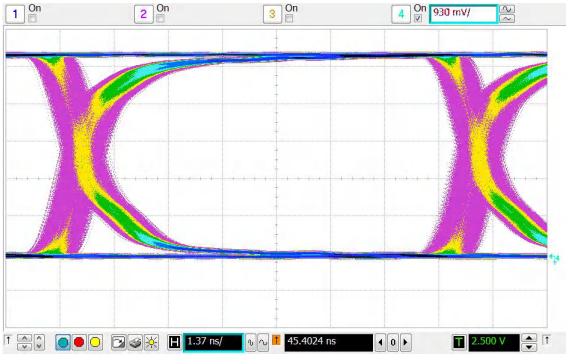


Figure 8-3. Eye Diagram at 100 Mbps PRBS, 5 V and 25°C

8.3 Power Supply Recommendations

To provide reliable operation at all data rates and supply voltages, a 0.1 µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors must be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501. For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 data sheet (SLLSEA0).

8.4 Layout

8.4.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 epoxy-glass as PCB material. FR-4 (Flame Retardant 4) meets the requirements of Underwriters Laboratories UL94-V0, and is preferred over cheaper alternatives due to the lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

8.4.2 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 8-4). Layer stacking must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of the inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links typically have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power / ground plane system to the stack to keep the planes symmetrical. This makes the stack mechanically stable and prevents warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see Application Note SLLA284, *Digital Isolator Design Guide*.

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8.4.3 Layout Example

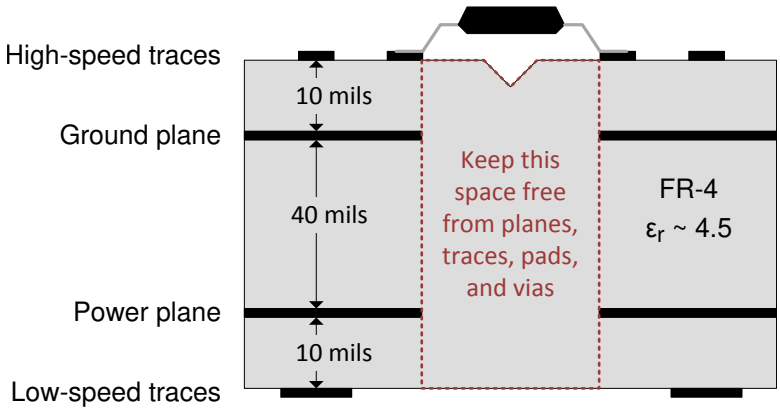


Figure 8-4. Layout Example

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9 Device and Documentation Support

9.1 Related Documentation

9.1.1 Related Documentation

See the *Isolation Glossary* (SLLA353)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (July 2022) to Revision H (November 2024)	Page
•	1
• Added content from the *High Voltage Feature Description* section to the *Specifications* section	4
• Moved the *IEC 60664-1 Ratings* table to the *Power Ratings* section in the *Specifications*	8
• Added typical specification to CPG/CLR in the *Insulation Specifications* section	8
• Moved the *Insulation Characteristics* table to the *Insulation Specifications* section	8
• Moved the *Package Insulation and Safety-Related Specification* table to the *Insulation Specifications* section	8
• Changed the *Regulatory Information Section* to the *Safety-related Certifications* section and moved to the *Specifications* section	11
• Moved the *Safety Limiting Values* to the *Specifications* section	12

Changes from Revision F (March 2016) to Revision G (July 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	1

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Changes from Revision E (December 2015) to Revision F (March 2016) **Page**

- Changed the Safety and Regulatory Approvals list of Section 1 1
- Added Section 1 "TUV Certification per EN 61010-1 and EN 60950-1" 1
- Changed text in the first paragraph of the *Section 3* From: "certifications according to VDE, CSA, and CQC". To: "certifications according to VDE, CSA, CQC, and TUV." 1
- Added Note 1 to Table 5-2 8
- Added TUV to the *Section 5.11* section and Table 5-4. Deleted Note 1 in Table 4 11
- Changed Figure 7-3 20

Changes from Revision D (July 2015) to Revision E (December 2015) **Page**

- Changed *Section 1* From: 8000V_{PK} V_{IOTM} and 2121 V_{PK} V_{IORM} Reinforced..To: 8000V_{PK} Reinforced..... 1
- Added Section 1: DW Package Certifications Complete; DWW Certifications Planned 1
- Added text to the Description: and extra-wide body (DWW) packages..... 1
- Added package: Extra wide SOIC, DWW (16) to the *Device Information* table 1
- Added the DWW pinout image 3
- Added the DWW package to the *Section 5.4* 5
- Changed the MIN value of CMTI in *Section 5.6* table From: 70 To: 100 kV/µs, deleted the TYP value of 100 kV/µs 6
- Added the DW package value to the Supply Current section of the *Section 5.6* 6
- Added the DWW package value to the Supply Current section of the *Section 5.6* 6
- Changed the MIN value of CMTI in *Section 5.7* table From: 70 To: 100 kV/µs, deleted the TYP value of 100 kV/µs 7
- Added the DW package value to the Supply Current section of the *Section 5.7* 7
- Added the DWW package value to the Supply Current section of the *Section 5.7* 7
- Changed the MIN value of CMTI in *Section 5.8* table From: 70 To: 100 kV/µs, deleted the TYP value of 100 kV/µs 8
- Added the DW package value to the Supply Current section of the *Section 5.8* 8
- Added the DWW package value to the Supply Current section of the *Section 5.8* 8
- Changed Parameter information and added the DWW package information in Table 5-1 8
- Added the DWW package to Table 5-3 8
- Changed C_{IO} typ value From: 2 To 1 pF in Table 5-3 8
- Added the DWW package to Table 5-2 8
- Added the DWW package information to Table 5-4 11
- added DWW-16 package options to Table 5-5 12
- Added t_{PHZ}, t_{PLZ}, t_{PZH}, and t_{PZL} to *Section 5.14* 13
- Added t_{PHZ}, t_{PLZ}, t_{PZH}, and t_{PZL} to *Section 5.15* 14
- Added Figure 6-2 16
- Changed Table 7-1 20
- Added text to the *Section 8.1* section: "isolation voltage per UL 1577." 21

Changes from Revision C (May 2015) to Revision D (July 2015) **Page**

- Added device ISO7821F to the data sheet 1
- Changed the *Section 3* to include: "default output is 'high' for the ISO7821 device and 'low' for the ISO7821F device. 1
- Changed the *Simplified Schematic* 1
- Changed Table 5-3 title From: *IEC Insulation and Safety-Related Specifications for DW-16 Package* To: *Package Insulation and Safety-Related Specifications* 8
- Changed Figure 5-1, Added Figure 5-2 12
- Changed t_{PLH} and t_{PHL} From: 5.5 V to 5 V in Figure 5-8 15
- Changed Figure 6-3 16

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- Changed the *Section 7.2* 18

Changes from Revision B (April 2015) to Revision C (May 2015) **Page**

- Changed From: V_{CC1} and V_{CC2} To: V_{CCI} and V_{CCO}, GND1 and GND2 To: GNDI and GNDO and added Notes 1 and 2 in the *Simplified Schematic* 1
- Changed the MIN value of CMTI in *Section 5.6* table From: 50 To: 70 kV/µs 6
- Changed the MIN value of CMTI in *Section 5.7* table From: 50 To: 70 kV/µs 7
- Changed the MIN value of CMTI in *Section 5.8* table From: 50 To: 70 kV/µs 8
- Changed the Installation classification of the Table 5-1 to include DW package information..... 8
- Added sentence "If the EN pin is available and low then the output goes to high impedance." to the *Section 7.1* section 18
- Changed the *Section 7.2* to include the EN pin on the Receiver side..... 18
- Changed "ISO782W functional modes" To: "ISO7821DW functional modes" in *Section 7.4* 20
- Changed Table 7-1 title From: "Functional Table" To: "ISO7821DW Function Table"..... 20
- Added the *Section 7.4.1* section 20
- Changed device number ISO7821 To: ISO7821DW in Figure 8-2 22

Changes from Revision A (December 2014) to Revision B (April 2015) **Page**

- Changed the document title From: "Channel Digital Isolator" To: "Channel 1/1 Digital Isolator" 1
- Added *Section 1*: 2.25V to 5.5V Level Translation..... 1
- Changed the Safety and Regulatory Approvals list of Section 1 1
- Changed text in the *Section 3* From: "This device is being reviewed for reinforced isolation certification by VDE and CSA. To: "This device has reinforced isolation certifications according to VDE, CSA, and CQC."..... 1
- Added Note (3) to the *Section 5.1* table..... 4
- Changed From: V_{CCX} To: V_{CCO} In I_{OH} and I_{OL} of the *Section 5.3* table 4
- Changed From: V_{CCX} To: V_{CCI} In V_{IH} and V_{IL} of the *Section 5.3* table 4
- Changed Note (1) of the *Section 5.3* table 4
- Changed From: V_{CCX} To: V_{CCO} In V_{OH} of the *Section 5.6* table 6
- Changed From: V_{CCX} To: V_{CCO} In $V_{I(HYS)}$ of the *Section 5.6* table 6
- Changed From: V_{CCX} To: V_{CCI} In I_{IH} of the *Section 5.6* table 6
- Changed From: V_{CCX} To: V_{CCI} In CMTI of the *Section 5.6* table 6
- Changed From: V_{CCX} To: V_{CCI} In Supply Current, DC Signal of the *Section 5.6* table..... 6
- Changed Note (1) of the *Section 5.6* table 6
- Changed From: V_{CCX} To: V_{CCO} In V_{OH} of the *Section 5.7* table 7
- Changed From: V_{CCX} To: V_{CCO} In $V_{I(HYS)}$ of the *Section 5.7* table 7
- Changed From: V_{CCX} To: V_{CCI} In I_{IH} of the *Section 5.7* table..... 7
- Changed From: V_{CCX} To: V_{CCI} In CMTI of the *Section 5.7* table 7
- Changed From: V_{CCX} To: V_{CCI} In Supply Current, DC Signal of the *Section 5.7* table 7
- Changed Note (1) of the *Section 5.7* table 7
- Changed From: V_{CCX} To: V_{CCO} In V_{OH} of the *Section 5.8* table 8
- Changed From: V_{CCX} To: V_{CCI} In I_{IH} of the *Section 5.8* table 8
- Changed From: V_{CCX} To: V_{CCI} In Supply Current, DC Signal of the *Section 5.8* table 8
- Changed Note (1) of the *Section 5.8* table 8
- Changed the Test Condition of CTI in Table 5-3 8
- Changed the MIN value of CTI From" > 600 V To: 600 V..... 8
- Changed Table 5-2 title From: *DIN V VDE 0884-10 (VDE V 0884-10) and UL 1577 Insulation Characteristics* To: *Added the DWW package to* 8
- Changed Table 5-2 8
- Changed columns VDE and CSA to Table 5-4 11
- Changed title From: *IEC Safety Limiting Values* To: *Section 5.12* 12

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- Changed the table in *Section 5.12*, added I_S DW-16 package options 12
- Changed Figure 5-1 12
- Changed Figure 6-1 16
- Changed From: V_{CC1} To: V_{CCI} in Figure 6-3 16
- Changed Figure 6-4 16
- Deleted INPUT-SIDE and OUTPUT-SIDE from columns 1 and 2 of Table 7-1 20
- Changed Note (1) of Table 7-1 20
- Changed the *Section 8.1* section 21
- Changed the *Section 8.2* section and Figure 8-1 21
- Added text and Figure 8-2 to the *Section 8.2.2* section 22

Changes from Revision * (November 2014) to Revision A (December 2014)	Page
• Changed From: A product preview that included only page 1 and the pinout section To: A complete data sheet	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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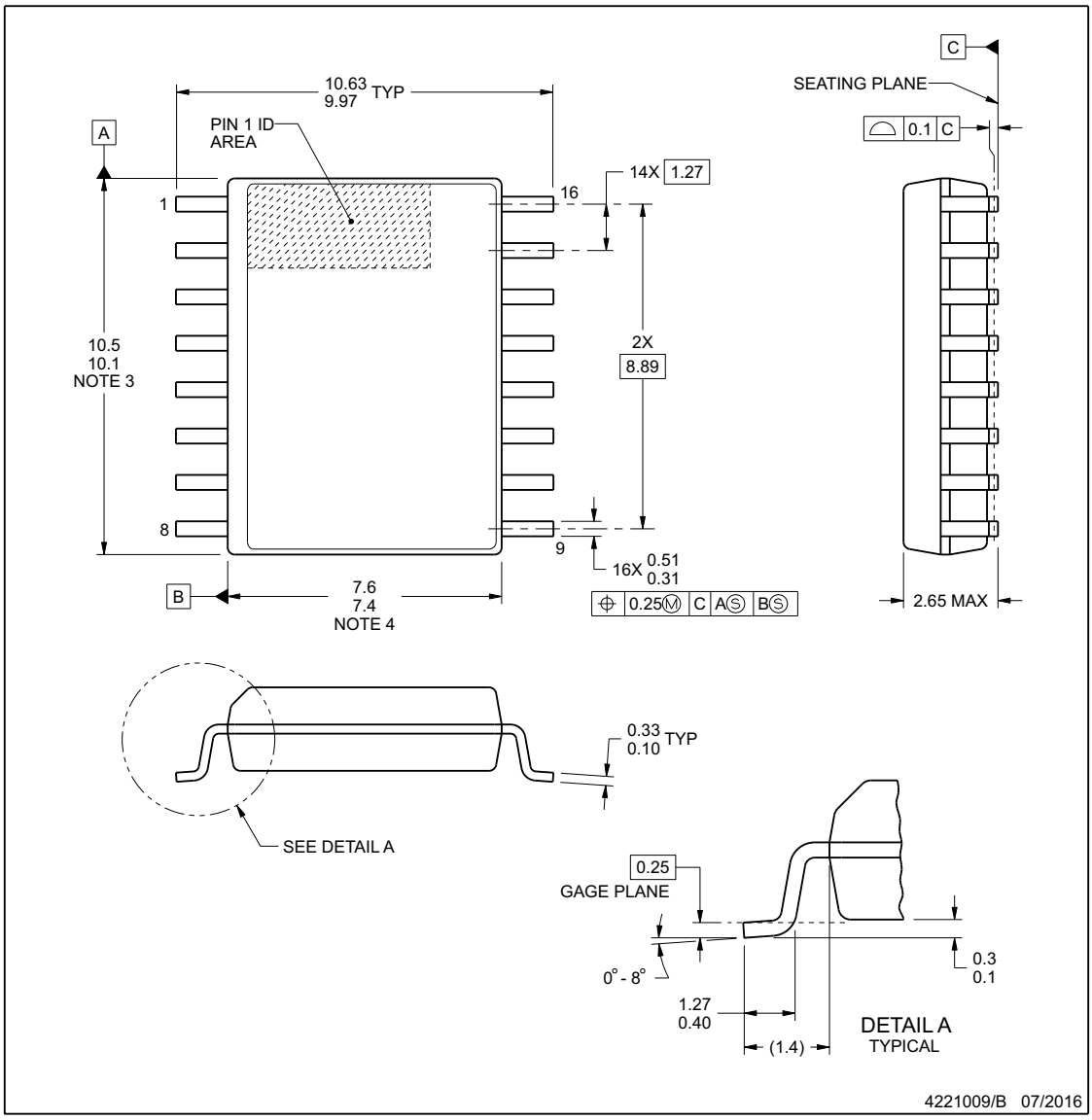


PACKAGE OUTLINE

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

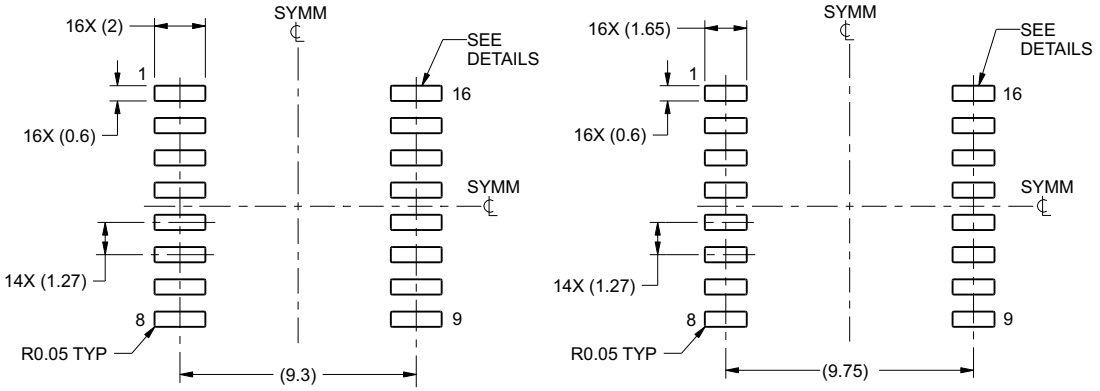
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EXAMPLE BOARD LAYOUT

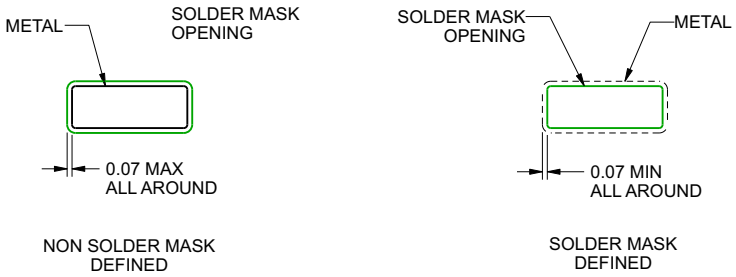
DW0016B

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:4X



SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

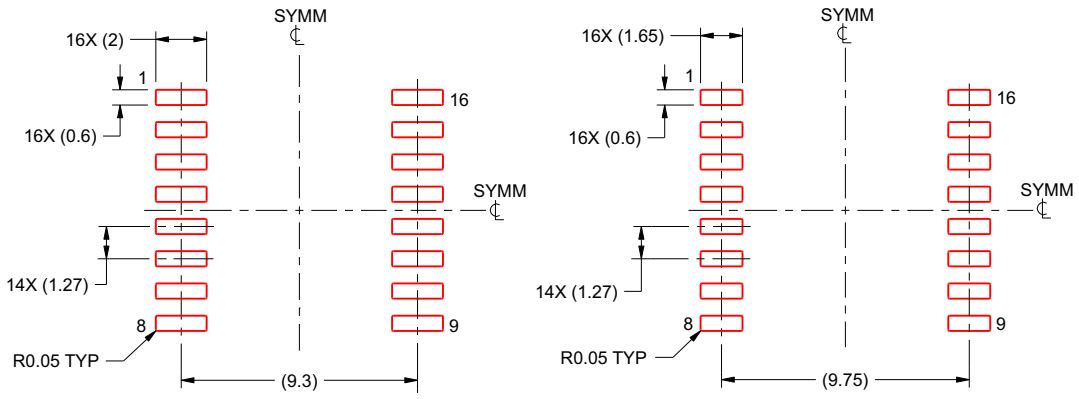
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EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

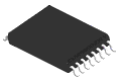
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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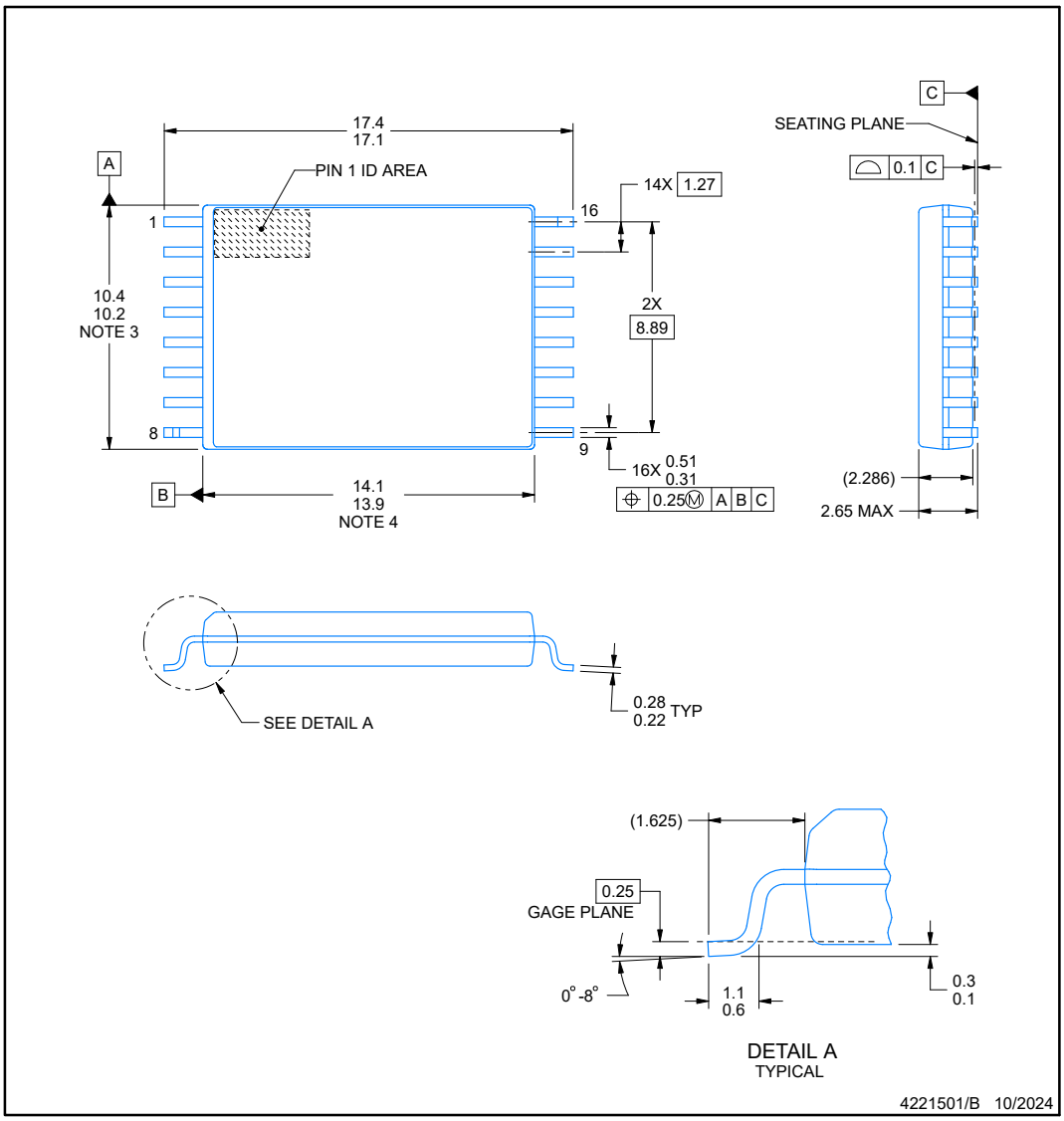
PACKAGE OUTLINE

DWW0016A



SOIC - 2.65 mm max height

PLASTIC SMALL OUTLINE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 mm per side.
4. This dimension does not include interlead flash.

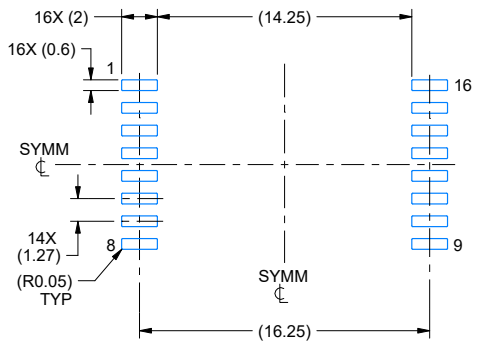
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EXAMPLE BOARD LAYOUT

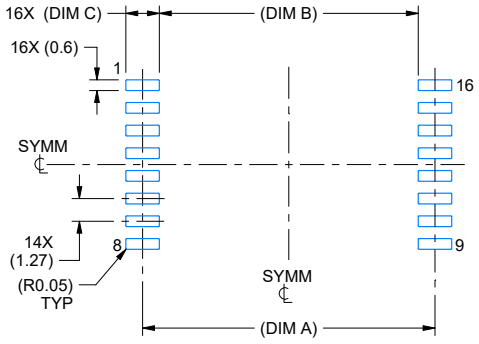
DWW0016A

SOIC - 2.65 mm max height

PLASTIC SMALL OUTLINE

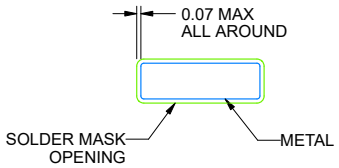


LAND PATTERN EXAMPLE
STANDARD
SCALE:3X

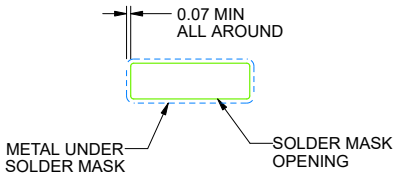


LAND PATTERN EXAMPLE
PCB CLEARANCE & CREEPAGE OPTIMIZED
SCALE:3X

OPTION	DIM A	DIM B	DIM C
01	16.375	14.5	1.875
02	16.625	15	1.625
03	16.725	15.2	1.525



NON SOLDER MASK
DEFINED
(PREFERRED)



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4221501/B 10/2024

NOTES: (continued)

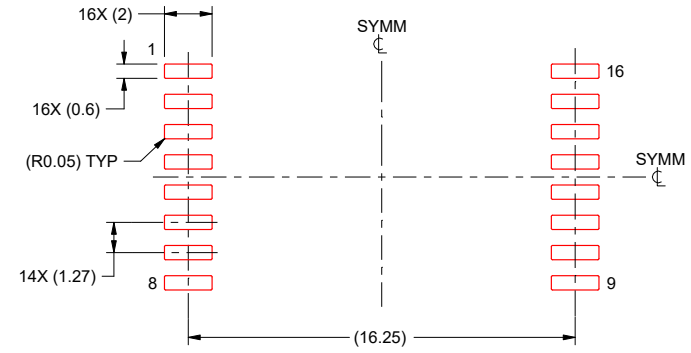
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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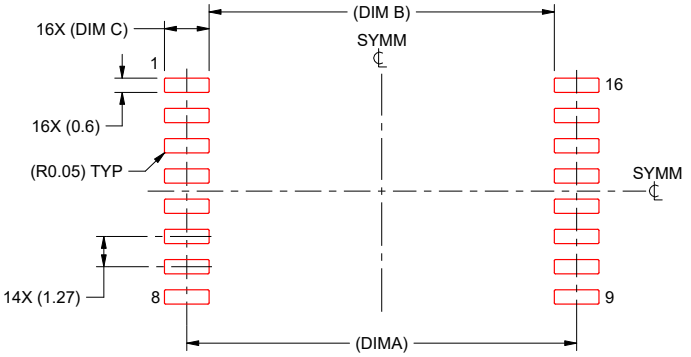
EXAMPLE STENCIL DESIGN

DWW0016A — **SOIC - 2.65 mm max height**

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
STANDARD
BASED ON 0.125 mm THICK STENCIL
SCALE:4X



SOLDER PASTE EXAMPLE
PCB CLEARANCE & CREEPAGE OPTIMIZED
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

OPTION	DIM A	DIM B	DIM C
01	16.375	14.5	1.875
02	16.625	15	1.625
03	16.725	15.2	1.525

4221501/B 10/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO7821DW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7821
ISO7821DW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7821
ISO7821DW.B	Active	Production	SOIC (DW) | 16	40 | TUBE	-	Call TI	Call TI	-55 to 125	
ISO7821DWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7821
ISO7821DWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7821
ISO7821DWR.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-55 to 125	
ISO7821DWW	Active	Production	SOIC (DWW) | 16	45 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	ISO7821
ISO7821DWW.A	Active	Production	SOIC (DWW) | 16	45 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	ISO7821
ISO7821DWW.B	Active	Production	SOIC (DWW) | 16	45 | TUBE	-	Call TI	Call TI	-55 to 125	
ISO7821DWWR	Active	Production	SOIC (DWW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	ISO7821
ISO7821DWWR.A	Active	Production	SOIC (DWW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	ISO7821
ISO7821DWWR.B	Active	Production	SOIC (DWW) | 16	1000 | LARGE T&R	-	Call TI	Call TI	-55 to 125	
ISO7821FDW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7821F
ISO7821FDW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7821F
ISO7821FDW.B	Active	Production	SOIC (DW) | 16	40 | TUBE	-	Call TI	Call TI	-55 to 125	
ISO7821FDWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7821F
ISO7821FDWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7821F
ISO7821FDWR.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-55 to 125	
ISO7821FDWRG4	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7821F
ISO7821FDWRG4.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7821F
ISO7821FDWRG4.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-55 to 125	
ISO7821FDWW	Active	Production	SOIC (DWW) | 16	45 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	ISO7821F
ISO7821FDWW.A	Active	Production	SOIC (DWW) | 16	45 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	ISO7821F
ISO7821FDWW.B	Active	Production	SOIC (DWW) | 16	45 | TUBE	-	Call TI	Call TI	-55 to 125	
ISO7821FDWWR	Active	Production	SOIC (DWW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	ISO7821F
ISO7821FDWWR.A	Active	Production	SOIC (DWW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	ISO7821F
ISO7821FDWWR.B	Active	Production	SOIC (DWW) | 16	1000 | LARGE T&R	-	Call TI	Call TI	-55 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

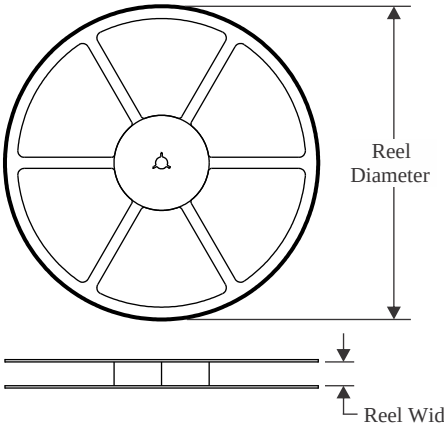
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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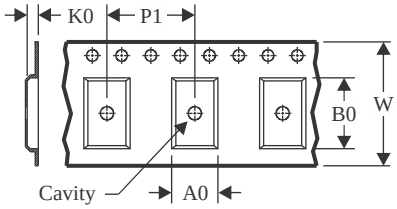
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

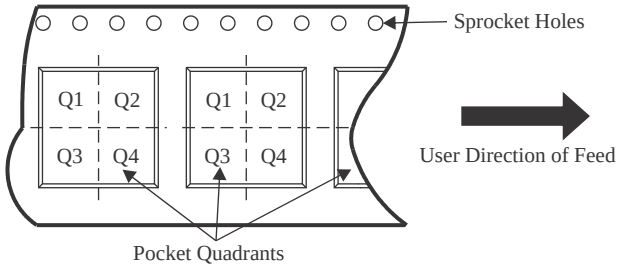


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

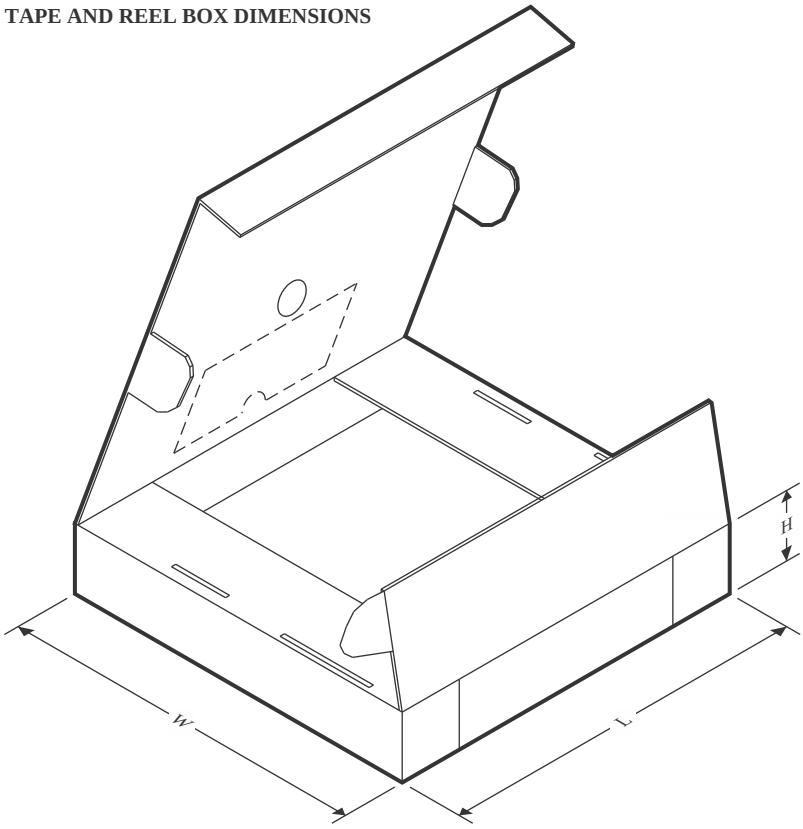
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7821DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7821DWWR	SOIC	DWW	16	1000	330.0	24.4	18.0	10.0	3.0	20.0	24.0	Q1
ISO7821FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7821FDWRG4	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7821FDWWR	SOIC	DWW	16	1000	330.0	24.4	18.0	10.0	3.0	20.0	24.0	Q1

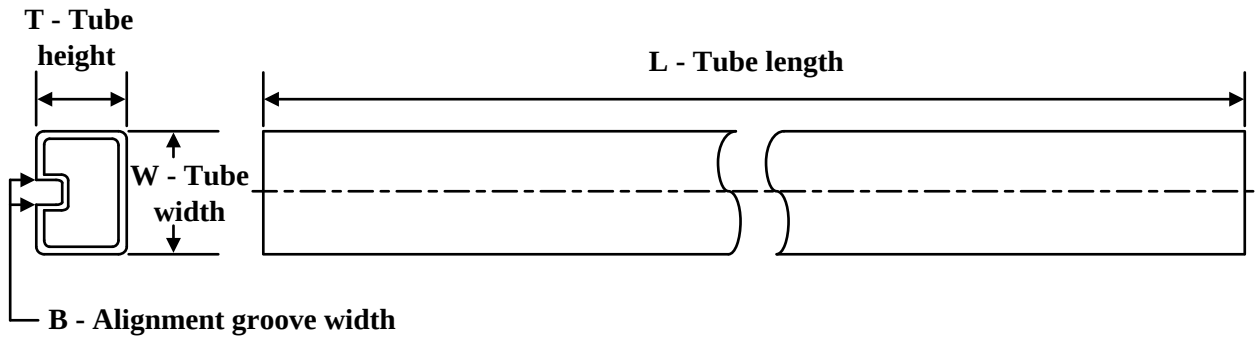
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7821DWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7821DWWR	SOIC	DWW	16	1000	350.0	350.0	43.0
ISO7821FDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7821FDWRG4	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7821FDWWR	SOIC	DWW	16	1000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO7821DW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7821DW.A	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7821DWW	DWW	SOIC	16	45	507	20	5000	9
ISO7821DWW.A	DWW	SOIC	16	45	507	20	5000	9
ISO7821FDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7821FDW.A	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7821FDWW	DWW	SOIC	16	45	507	20	5000	9
ISO7821FDWW.A	DWW	SOIC	16	45	507	20	5000	9

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